Introduction of TLP (Transmission Line Pulse) for ESD Analysis and Applications - Summary

ESDEMC

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Outline

1. ESD Background

2. TLP Testing Techniques Introduction

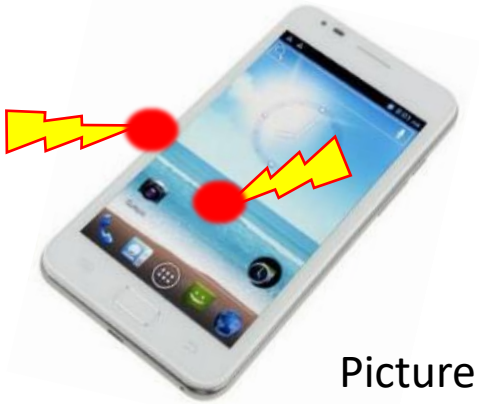
3. TLP Testing Application

4. TLP System Configuration Considerations

What is ESD?

- Electrostatic Discharge (ESD) is an exchange of charge between two objects, It occurs when contact is established or if the dielectric breakdown of the material between the two objects is exceeded.

Picture 1



Picture 2

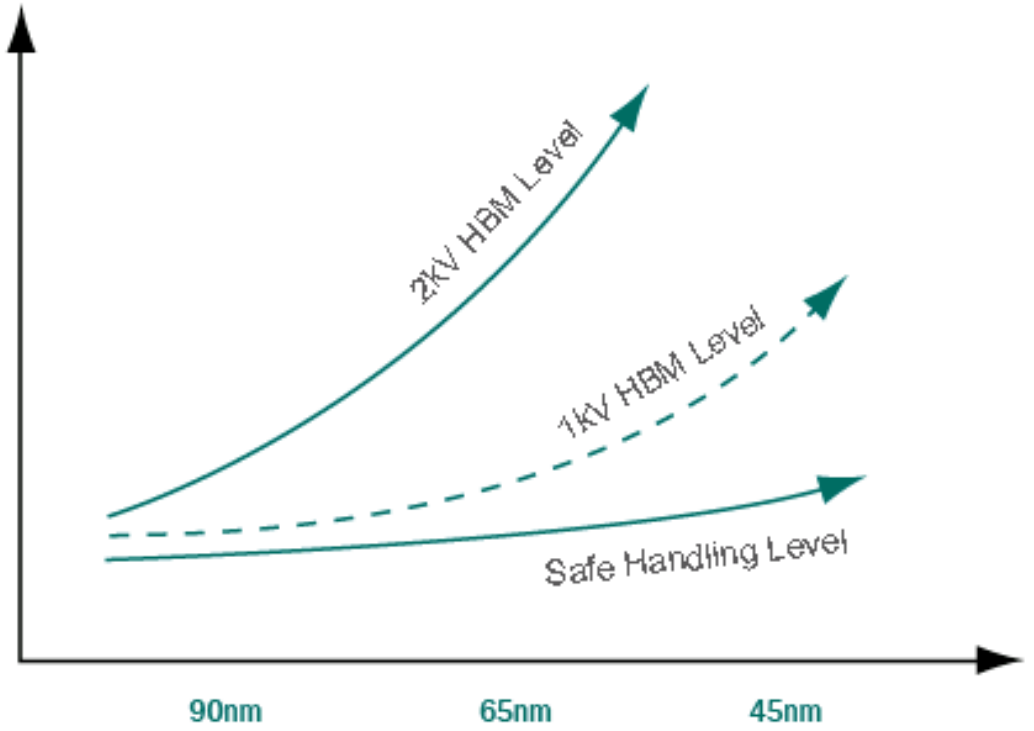
Table 1: Static Voltage Generation Examples (Source: ESD Association)

Examples of Static Voltage Generation At Different Levels of Relative Humidity (RH)		
Means of Generation	10-25% RH	65-90% RH
Walking across carpet	35,000 V	1,500 V
Walking across vinyl tile	12,000 V	250 V
Worker at bench	6,000 V	100 V
Poly bag picked up from bench	20,000 V	1,200 V
Chair with urethane foam	18,000 V	1,500 V

Note: The voltages are relatively high, some of them may occur under some extreme cases.

Why do we care about ESD?

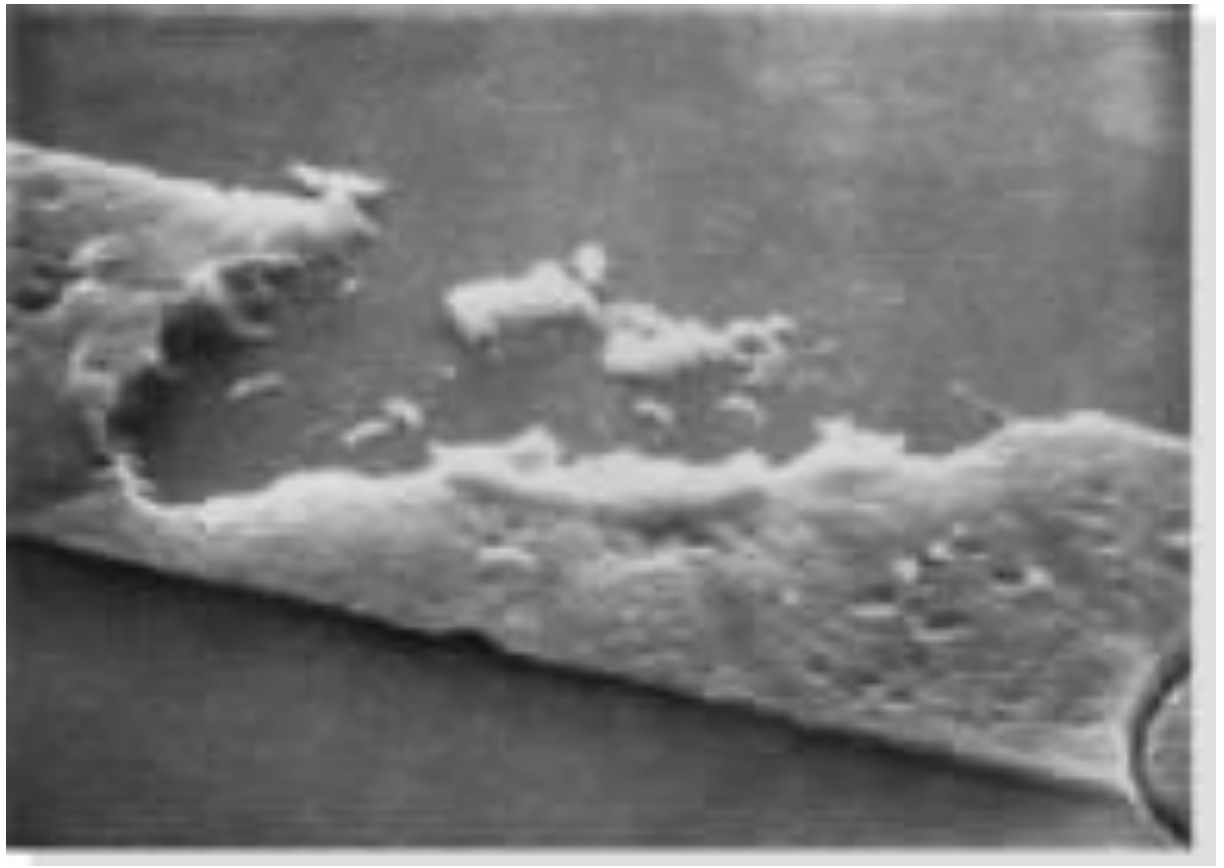
Cost of ESD design dependent on
- chip area
- respins
- resources
- circuit performance
- time-to-market



Source: 2005 ESD/EOS Symposium paper

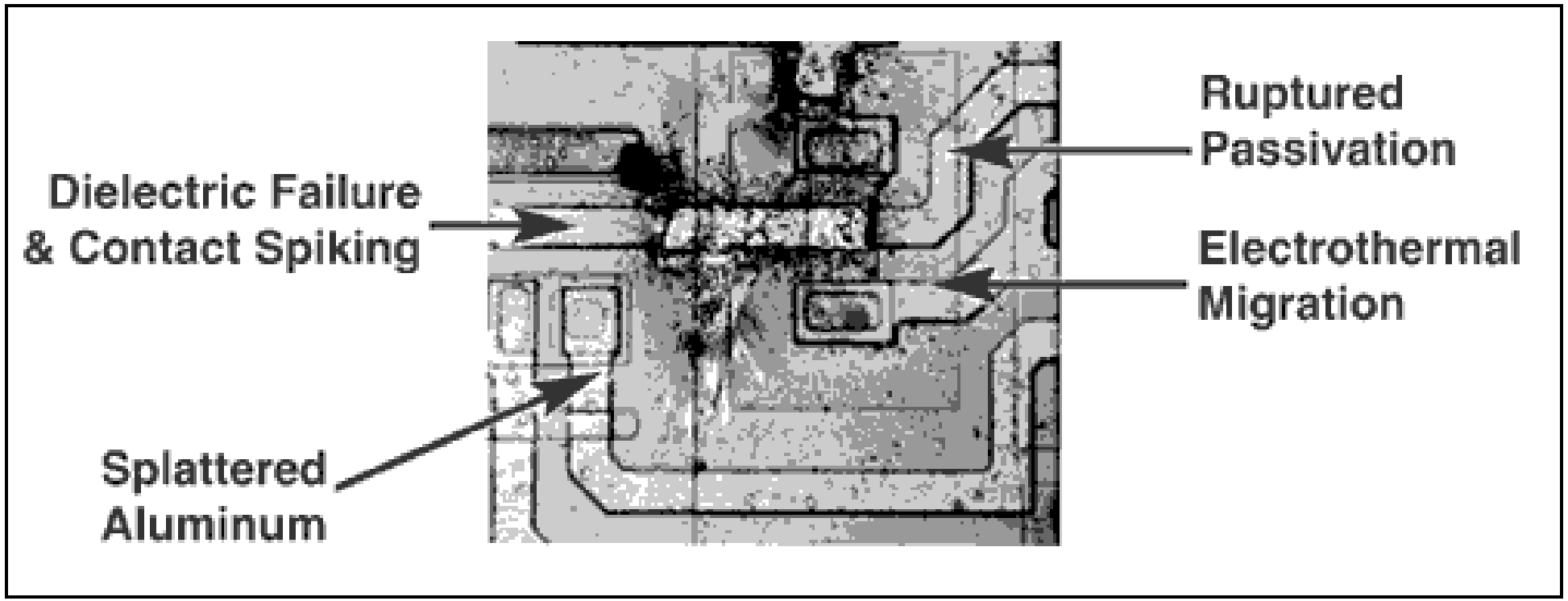
- Potential damage to circuit designs, leading to:
  - Poor product quality
  - Disappointed customers
  - Increased costs for repair and rework
- Components permanent damage by breakdown, or oxide punch through, excessive local heating as components may not be able to dissipate the energy fast enough.

Physical Damage, Still Functional - IC Damages from ESD



Picture 1: ESD overvoltage surge. Still operable but close to total failure.

Hard failure - IC Damages from ESD



Picture 2: RS-232 interface IC after an ESD strike of 15kV

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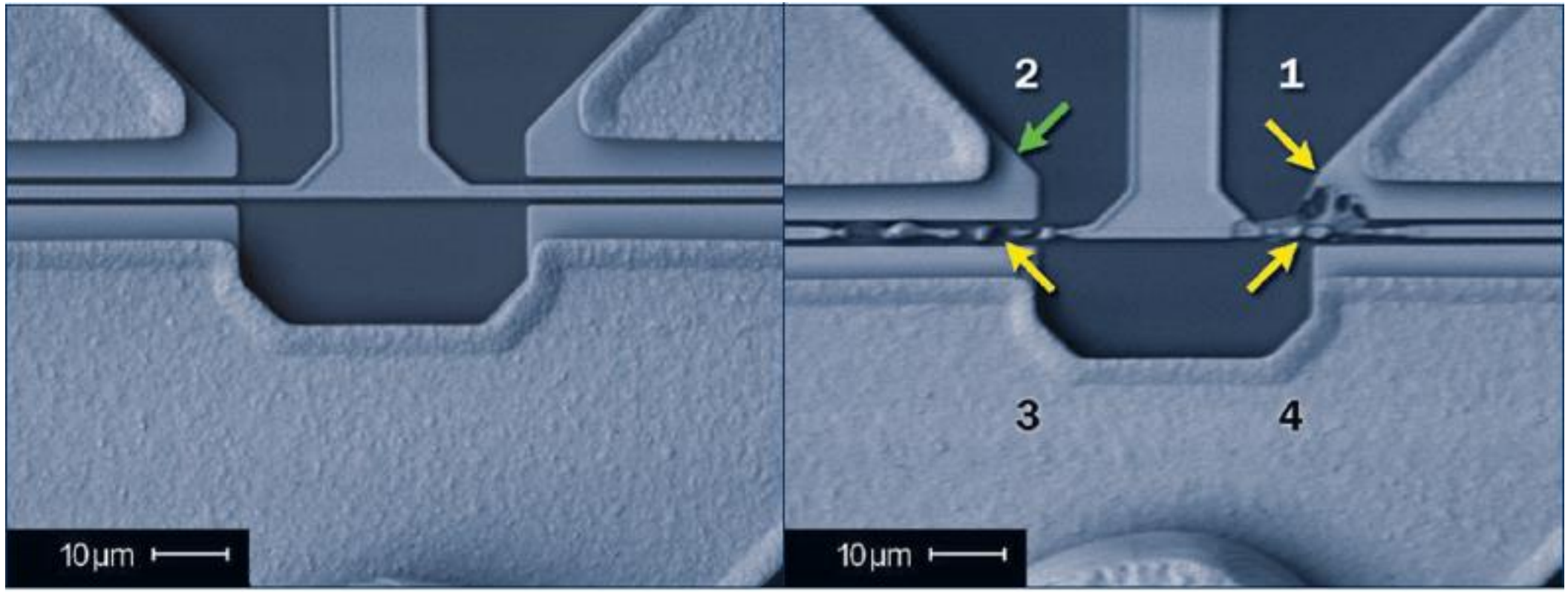
Hard failure - IC Damages from ESD



Shown on the left is a SEM image of good transistor. To the right is a SEM image showing EOS damage (indicated by yellow arrows).

Picture 3: EOS (Electrostatic Over Stress) damage

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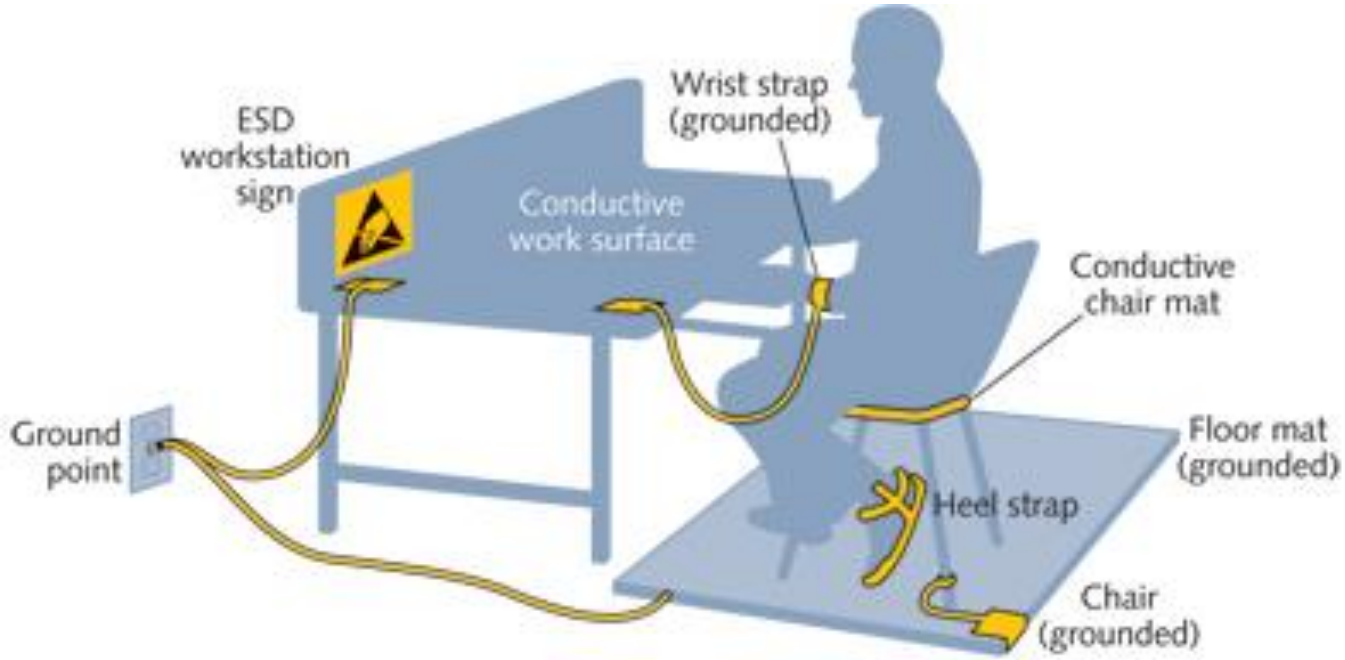
How to protect against ESD?

1. Controlled Environment

- Reduce the potential for charge build up
- Grounded equipment and furniture
- Clean Room - Controlled humidity and particles
- Does not help when system is shipped to End-User, such as **Consumer Electronics**



Picture 4: ESD Friendly Workspace

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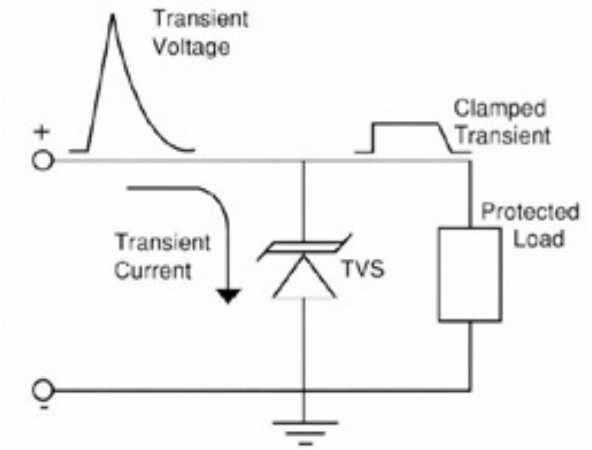
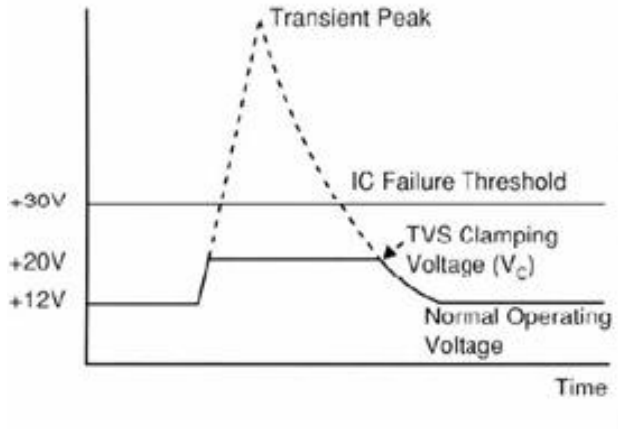
How to protect against ESD?

2. Improve System ESD Robustness

- Understand system working environment and potential ESD risks
- Design your system with careful ESD protection strategy !
  (Please refer to System Level ESD - White Paper 1,2,3 - Industry Council on ESD Target Levels, http://esda.org/IndustryCouncil.html)
  - ✓Understand ESD sensitivities of critical components
  - ✓Test and choose best ESD protection solutions for weakness
  - ✓Test and further improve system level ESD robustness
- Design engineers need critical data from different types of ESD tests.
- TLP test is a very powerful tool that provides many important data for ESD design !





Graph 1

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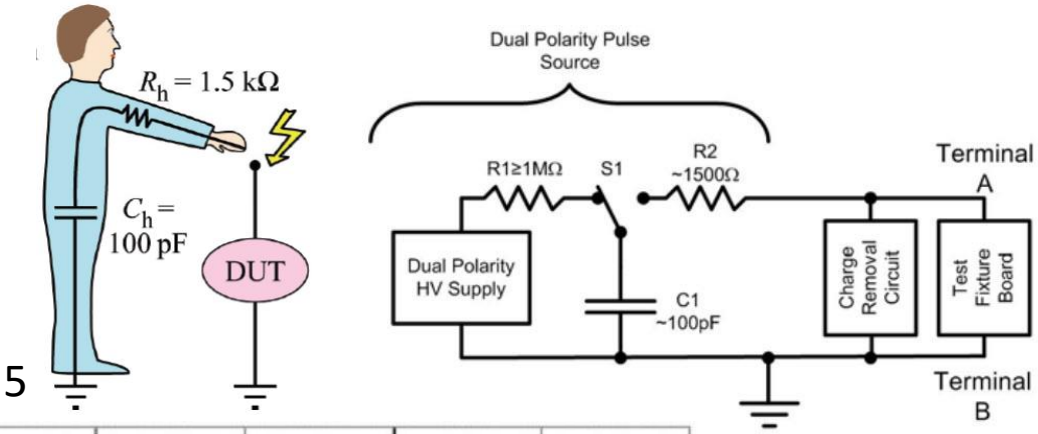
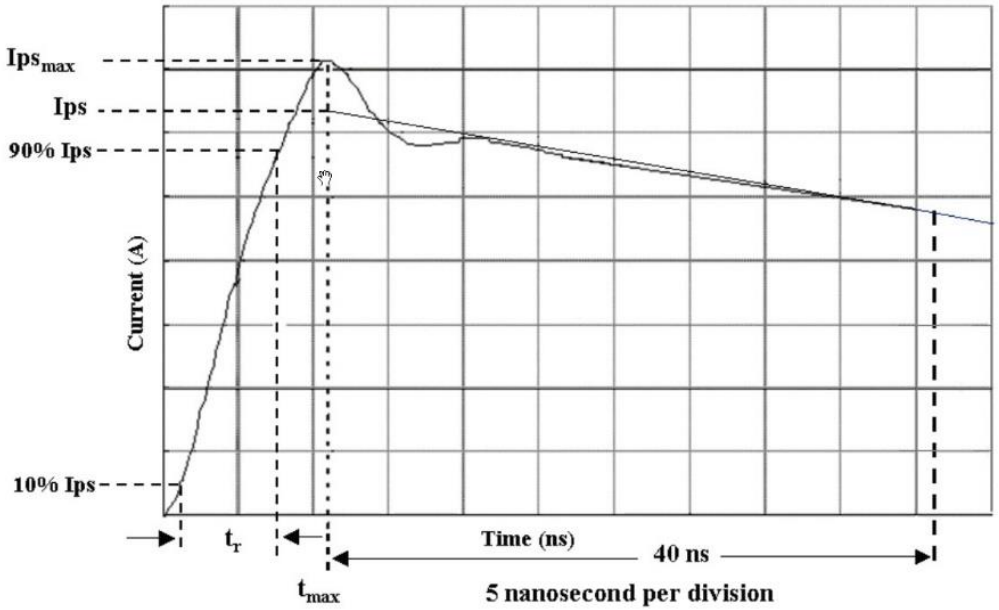
How to test for ESD robustness?

1. Human Body Model (HBM) [2]

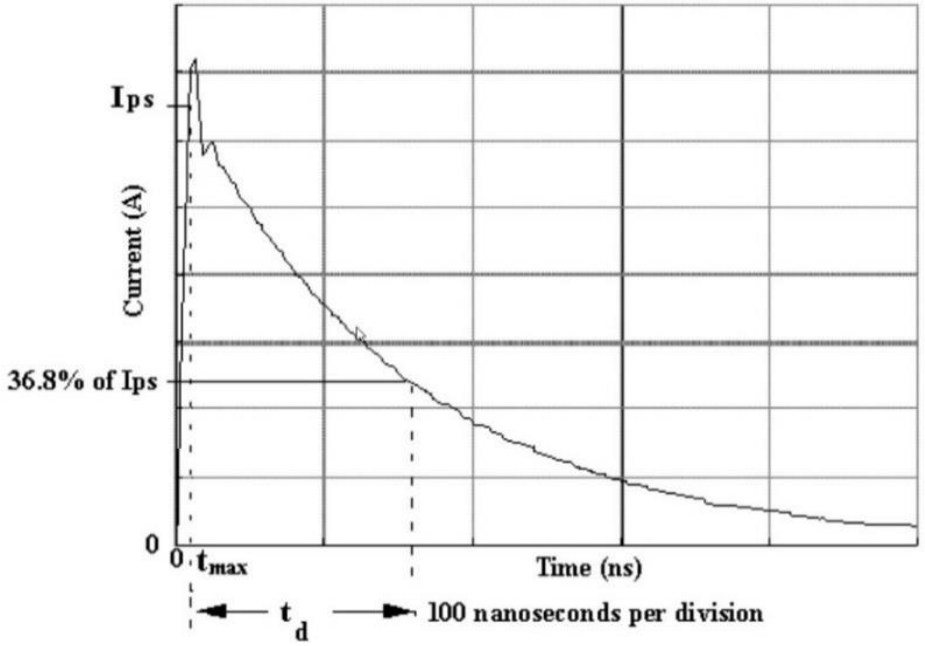
- Charged human body contact with device under test (DUT)
- ANSI/ANSI/ESDA/JEDEC JS-001-2017
- Classify up to 4 kV, < 3A into a short (8 kV optional)
- Discharge from the skin



Picture 5



Rise Time (t_r) for short : 2 to 10ns



Decay Time (t_d) for short : 130 to 170ns

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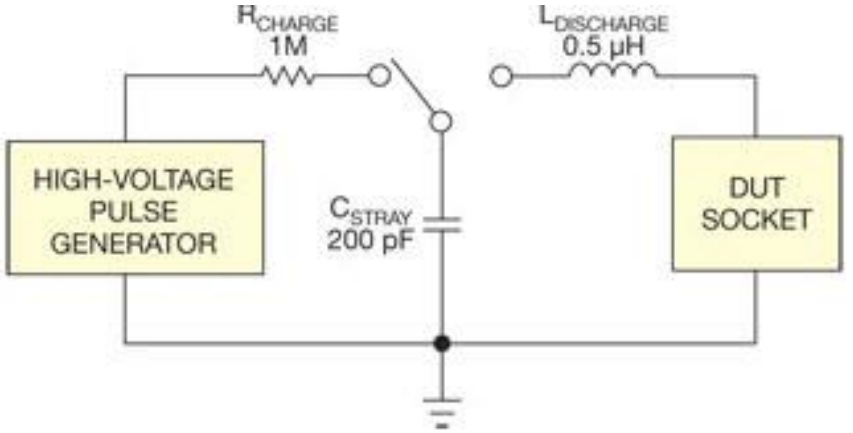
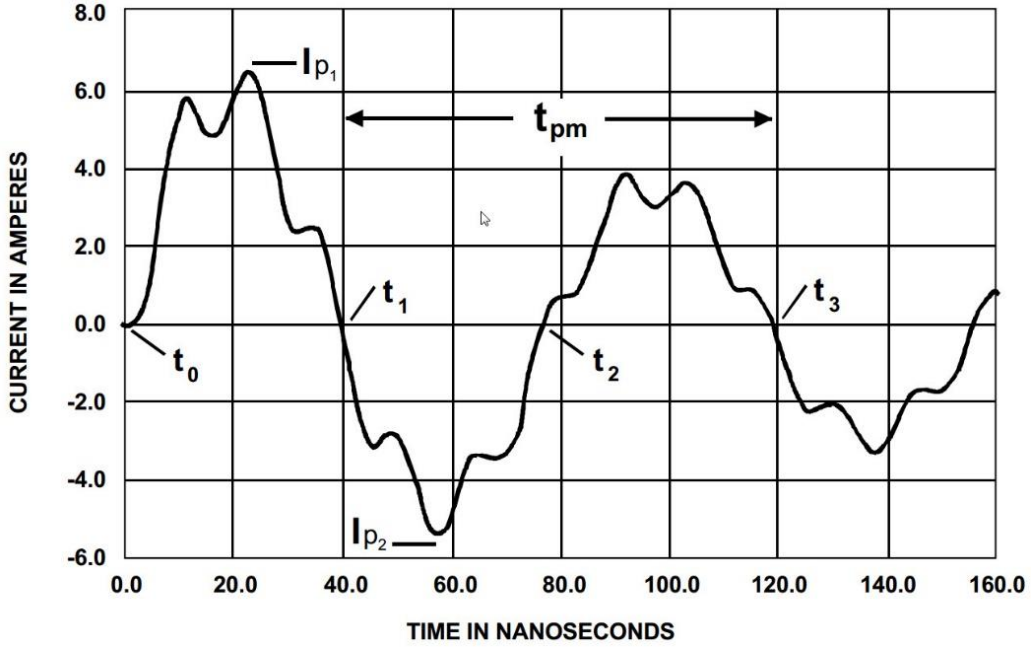
How to test for ESD robustness?

2. Machine Model (MM) [3]

- Charged machine discharge to devices, such as during production
- ESD STM5.2-2012 – obsoleted, then SP5.2-2019
- Classify up 400 V
- < 7A into a short
- MM model is rarely used



Graph 2



Major Pulse Period (t_{pm}) for short : 66 to 90ns

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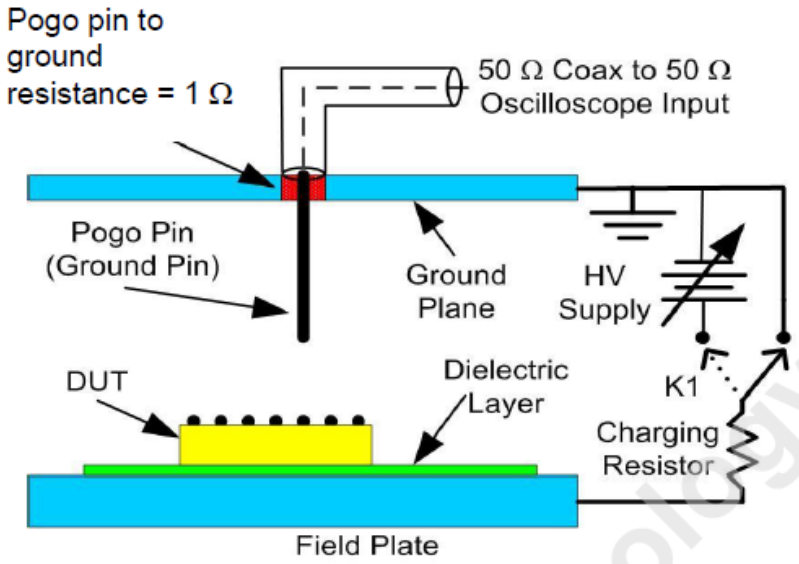
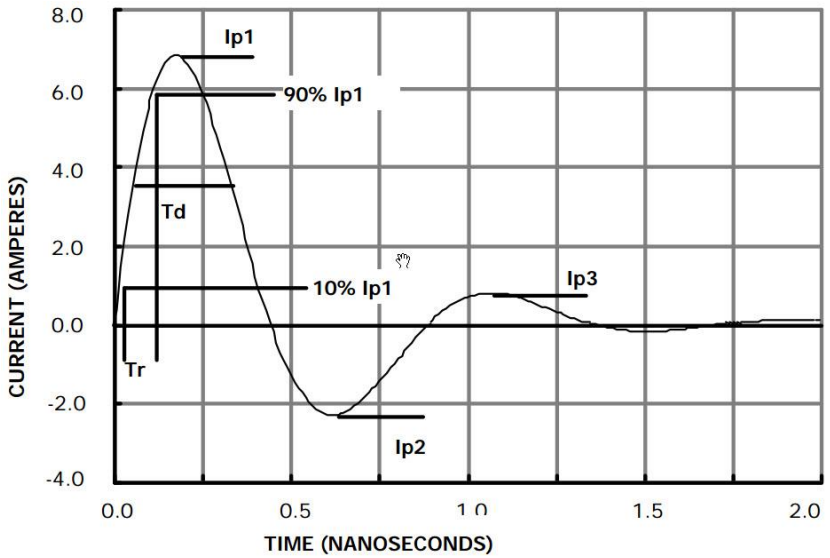
How to test for ESD robustness?

3. Charged Device Model (CDM) [4]

- Charged device discharge to other metal parts or ground plane, such as an IC during assembly
- ANSI/ESDA/JEDEC JS-002-2018
- Device is charged via a charging plate
- Non-contact discharge as grounded object approaches a charged pin
- Classify up to 2000V
- 30A@1 kV (4pF verification module, <260ps rise time)



FI-CDM setup (JS-002-2018)



Rise Time (t_r) : ~200ps, Full Width Half Height (t_d) : ~400ps

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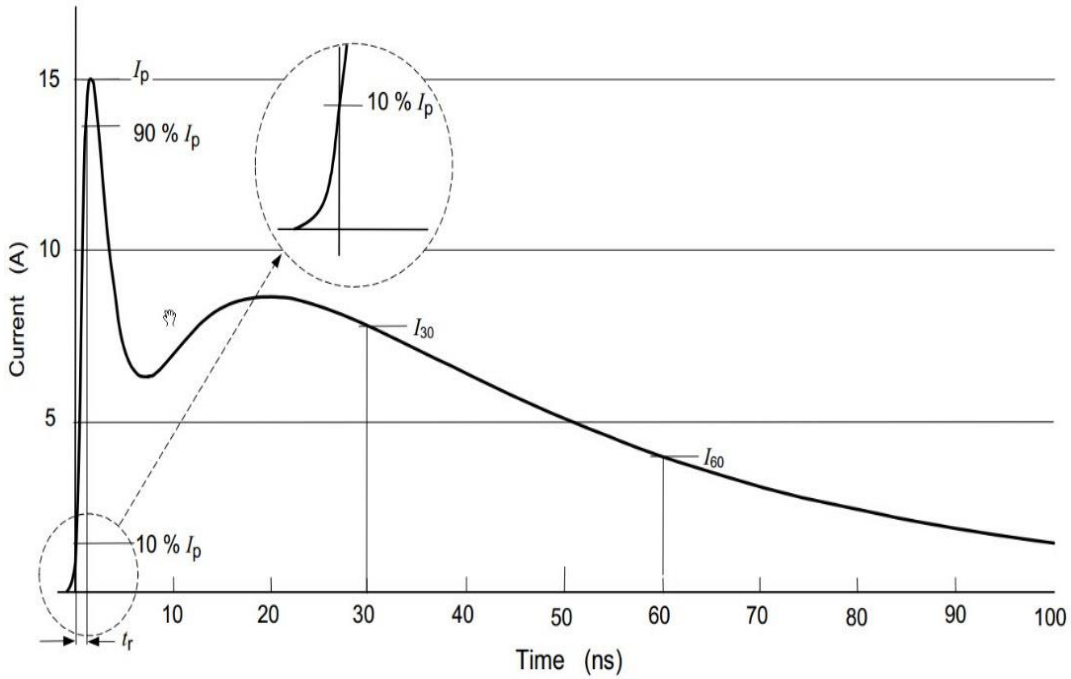
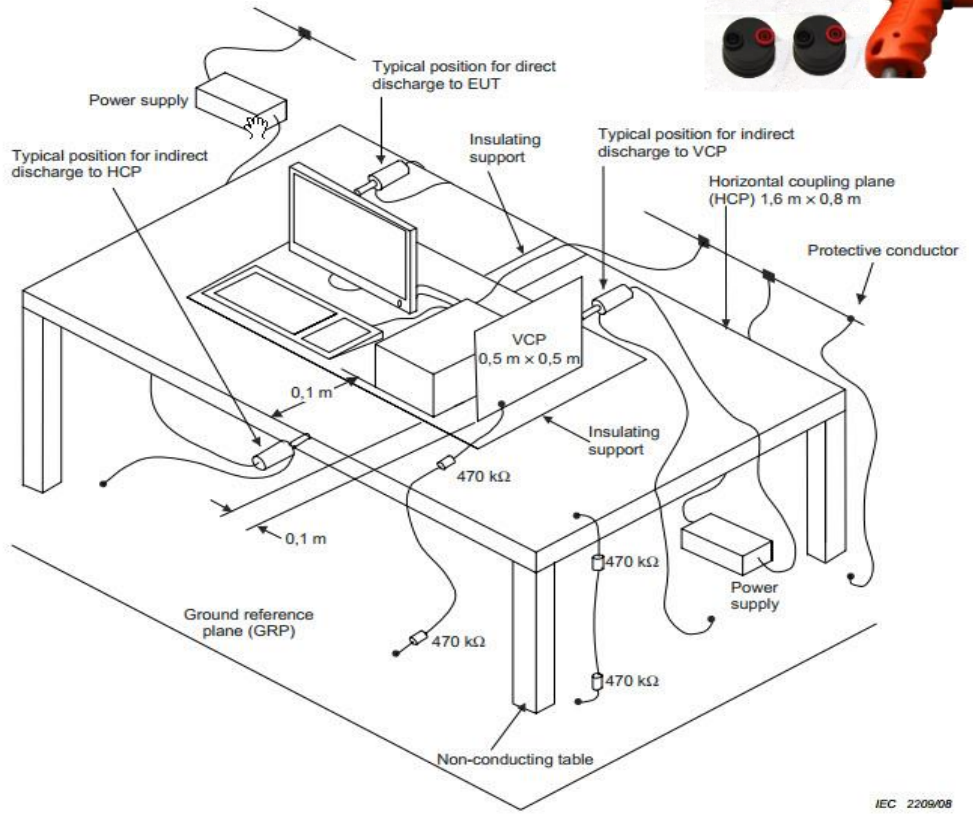
How to test for ESD robustness?

4. Human Metal Model (HMM) [5]

- Charged human body contacting a DUT with a metal, discharging to a system
- IEC 61000-4-2: 2008
- System level test



Ideal contact discharge waveform (4kV)



IEC Test Configuration

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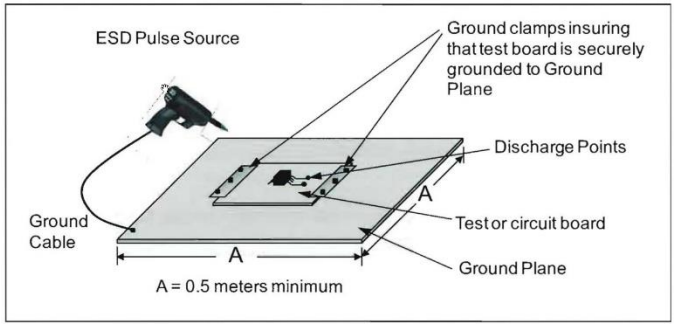
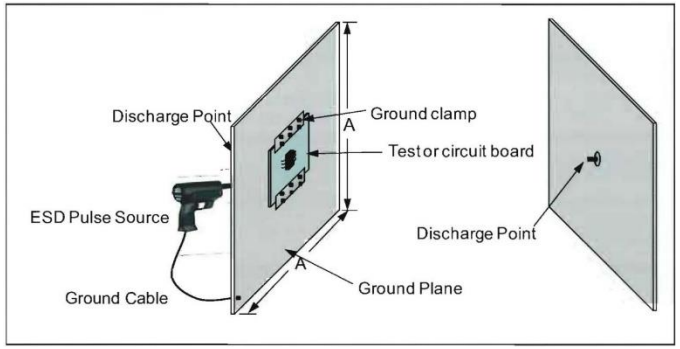
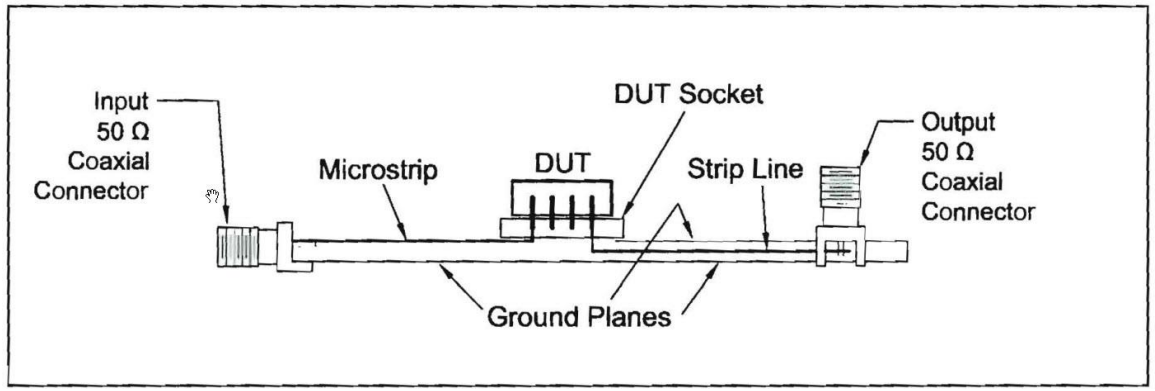
How to test for ESD robustness?

4. Human Metal Model (HMM) [6]

- Charged human discharging through a metal tool
- ANSI/ESD SP5.6-2009
- Component level test similar to IEC 61000-4-2
- Current waveform parameters same as IEC 61000-4-2
- Can use TLP and the 50W arrangement for more reliable and automatic failure detection testing







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TLP testing introduction

- **Transmission-Line Pulse (TLP) Testing** is a methodology to test, and study integrated circuit technologies and circuit behavior in the time domain of transient events, such as Electrostatic-Discharge (ESD), Cable Discharge Event (CDE) .

- **History:**
  - Due to interest in Electromagnetic Pulse environments, Wunsch and Bell studied **pulsed power failures in semiconductor junctions** in the 1960's. [7]
  - Also developed in the 1960's, by Bradley, Higgins et.al., was the use of charged transmission lines to generate rectangular pulses [8]
  - In the 1980's the idea of using Transmission Line Pulsing for modeling of ESD phenomena was introduced by Maloney and Khurana [9]
  - The first commercial TLP system was introduced in the mid-1990's [10]

TLP testing standards

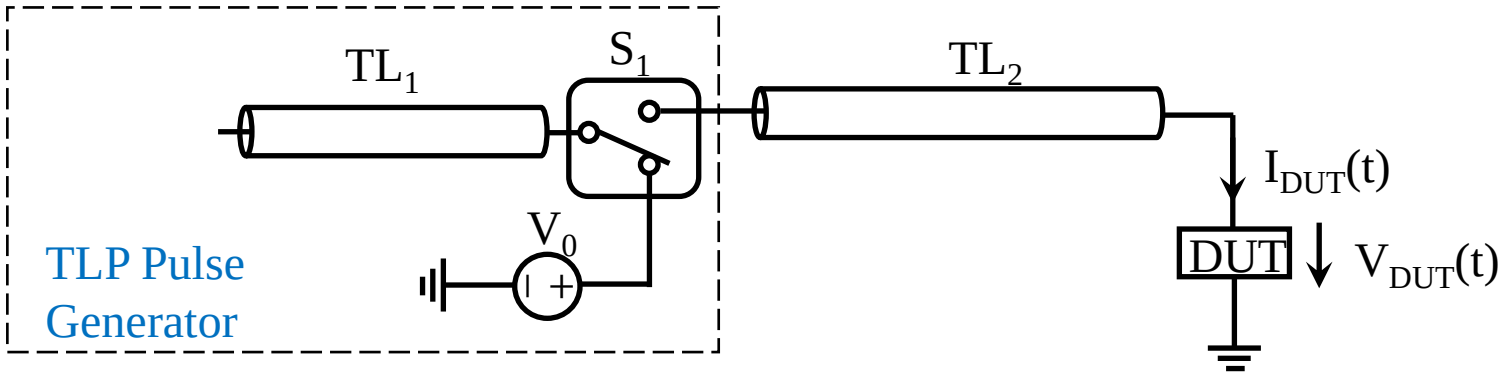
[1] ANSI/ESD STM5.5.1-2022 For Electrostatic Discharge Sensitivity Testing - Transmission Line Pulse (TLP) - Device Level

[2] IEC 62615:2010 Electrostatic Discharge Sensitivity Testing – Transmission Line Pulse (TLP) – Component Level

- **Standard TLP**
  - **Pulse Width** > 10ns (typical value: 100ns)
  - 20%-80% **Rise Time** ≤ 10% pulse width
  - Minimum of 200MHz BW voltage probe
  - Minimum of 200MHz BW current probe
  - Minimum of 200MHz BW oscilloscope
- **Very Fast TLP (VF-TLP)**
  - **Pulse Width** ≤ 10ns
  - 20%-80% **Rise Time** ≤ 10% pulse width
  - Minimum of 1GHz BW voltage probe
  - Minimum of 2GHz BW current probe
  - Minimum of 2.5GHz BW oscilloscope

TLP testing introduction

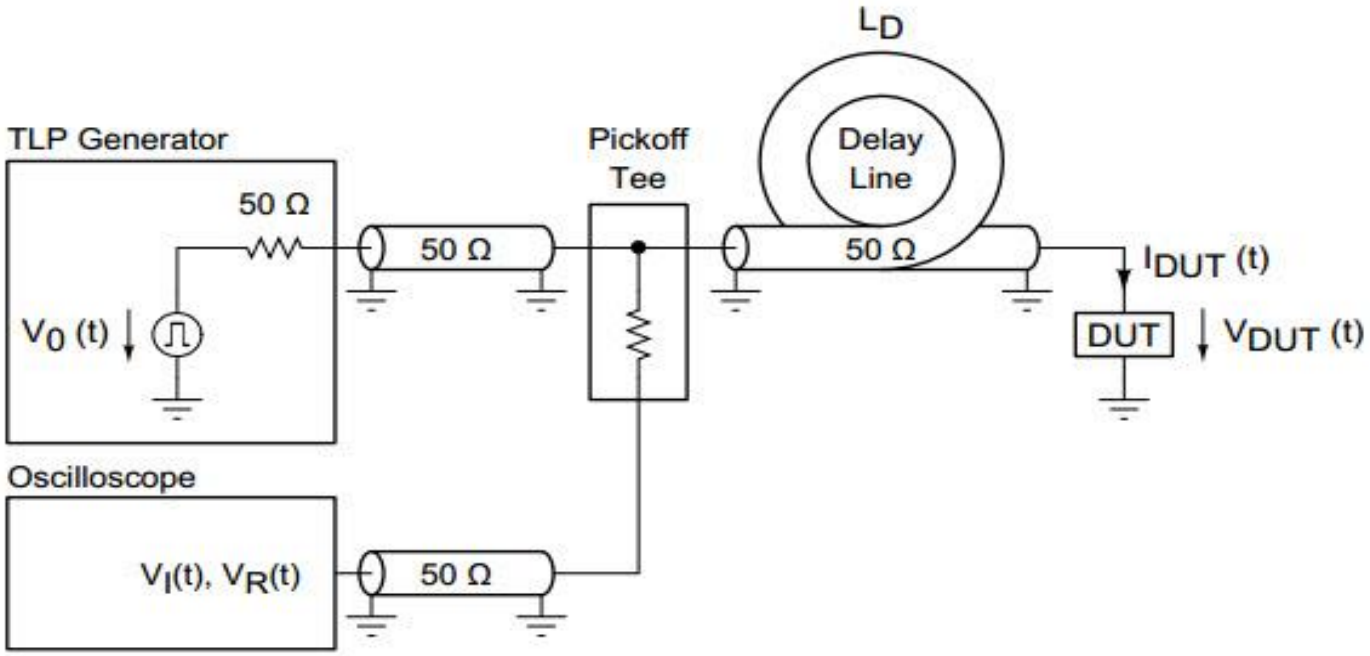
- A basic TLP pulse generator consists of a charge line (TL1) of length L, a switch (S1), and a High Voltage power supply (Vo)



- The length of the charge line TL_1 determines the TLP pulse width
- Standard TLP typically uses 100ns pulse width
- Pulse level will be incrementally increased until failure obtain, or reached the maximum voltage
- Failure typically determined by DC leakage current change

VF-TLP testing introduction

- Commonly used for characterizing device **clamping speed** and **voltage overshoot**
- Narrow pulse width ($\leq$ 10ns)
- Time Domain Reflection Separate (TDR-S) setup is usually used for VF-TLP measurement setup. Incident and reflected pulses can be measured separately and precisely by a long low loss delay line with wide-bandwidth voltage pick-up Tee
- De-embedding of the measurement cable and probe loss is necessary and performed using frequency domain techniques



A Typical VF-TLP Measurement Setup with Delay Line

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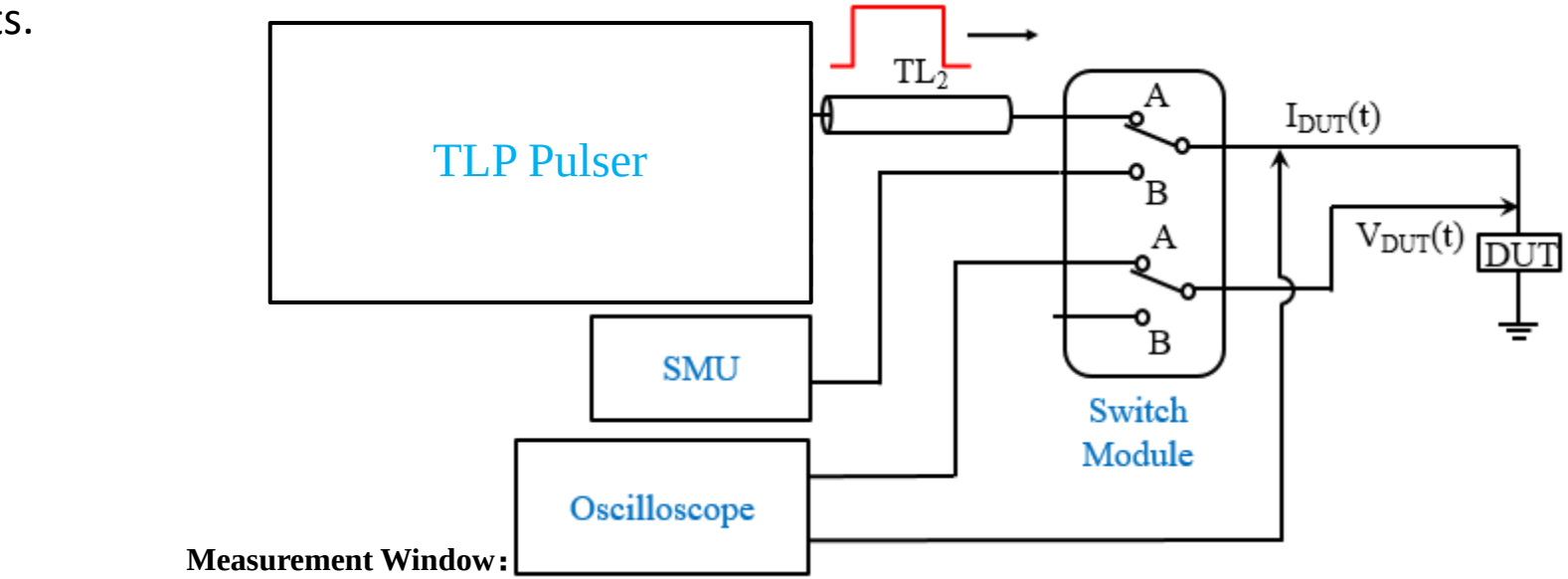
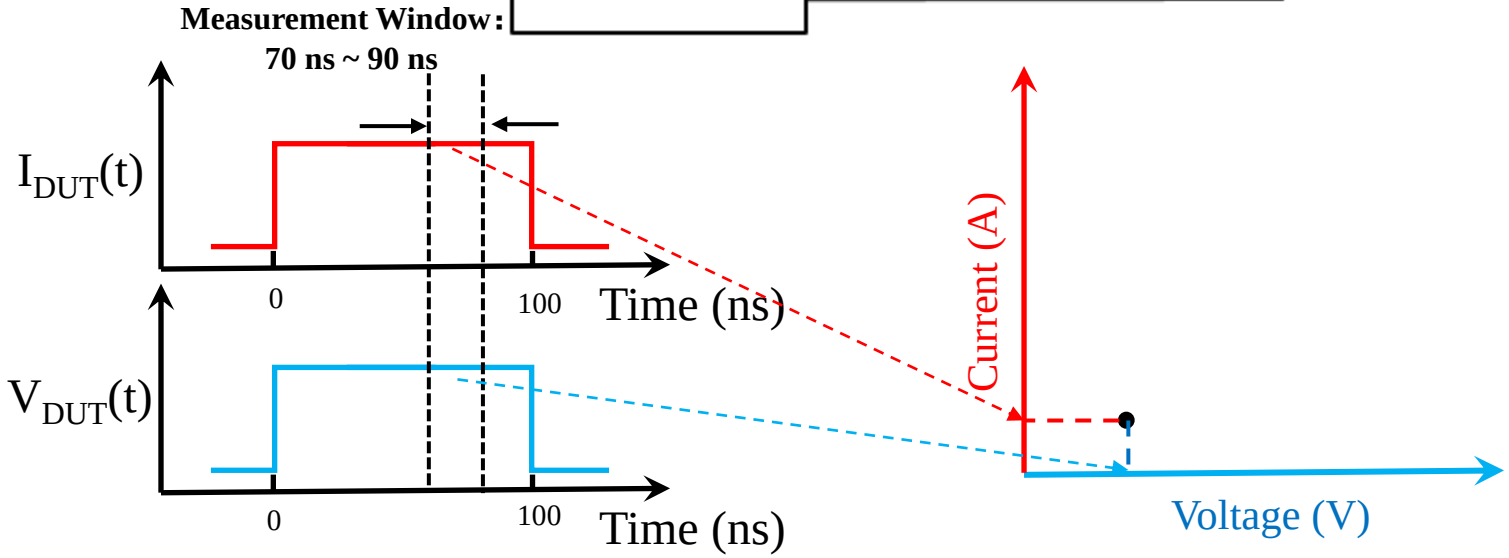
TLP testing IV & Leakage curves obtain

Step 1-A：

Both switches of the Switch Module are set to terminal A. TLP Pulser discharge to the DUT via TL_2. The oscilloscope capture $I_{DUT}(t)$ and $V_{DUT}(t)$ waveforms. The data withing the 70% - 90% pulse duration is averaged to obtain a pair of (I, V) points.





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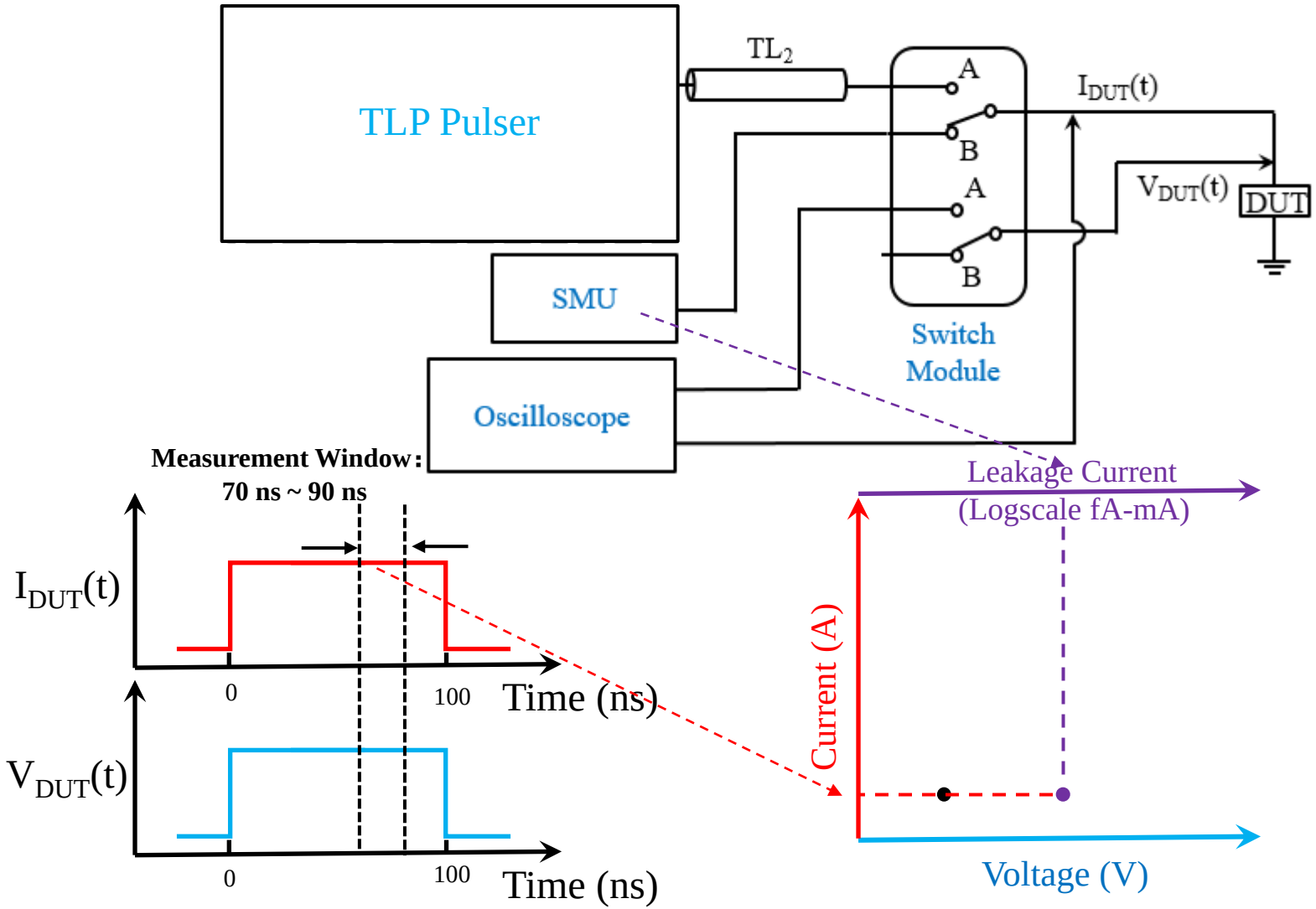
TLP testing IV & Leakage curves obtain

Step 1-B：

Both switches of the Switch Module are set to terminal B, measure leakage current by SMU.



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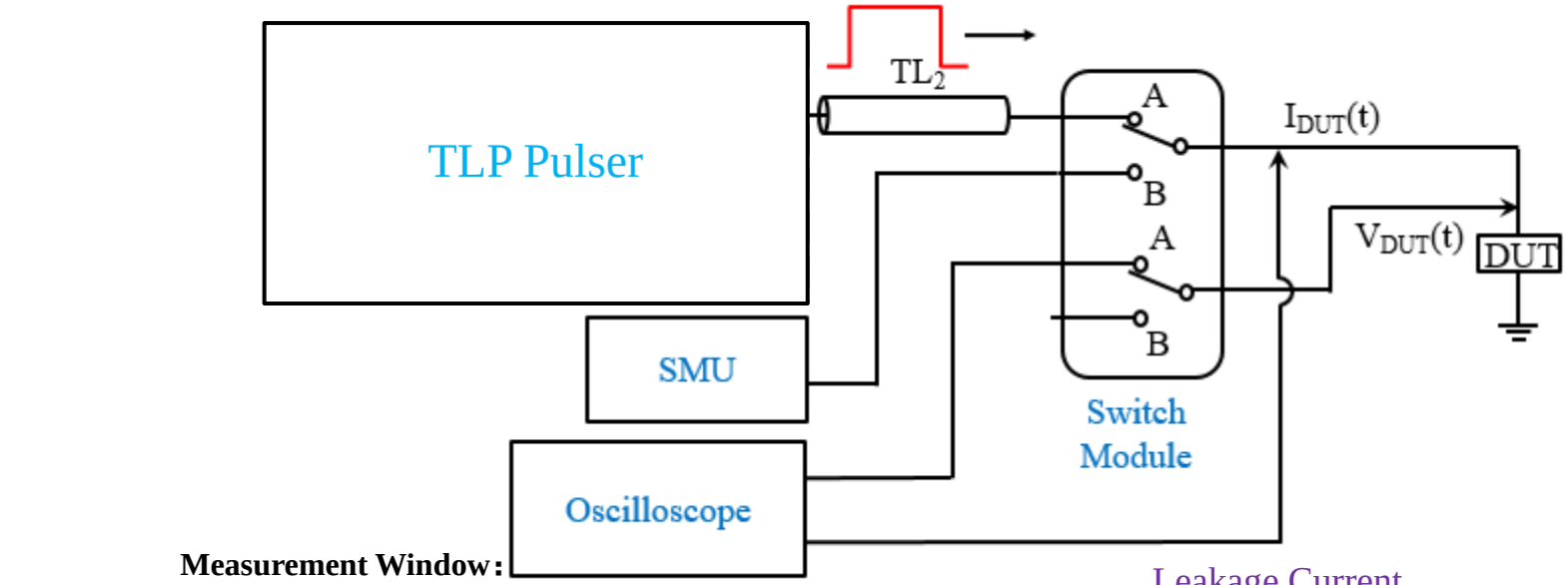
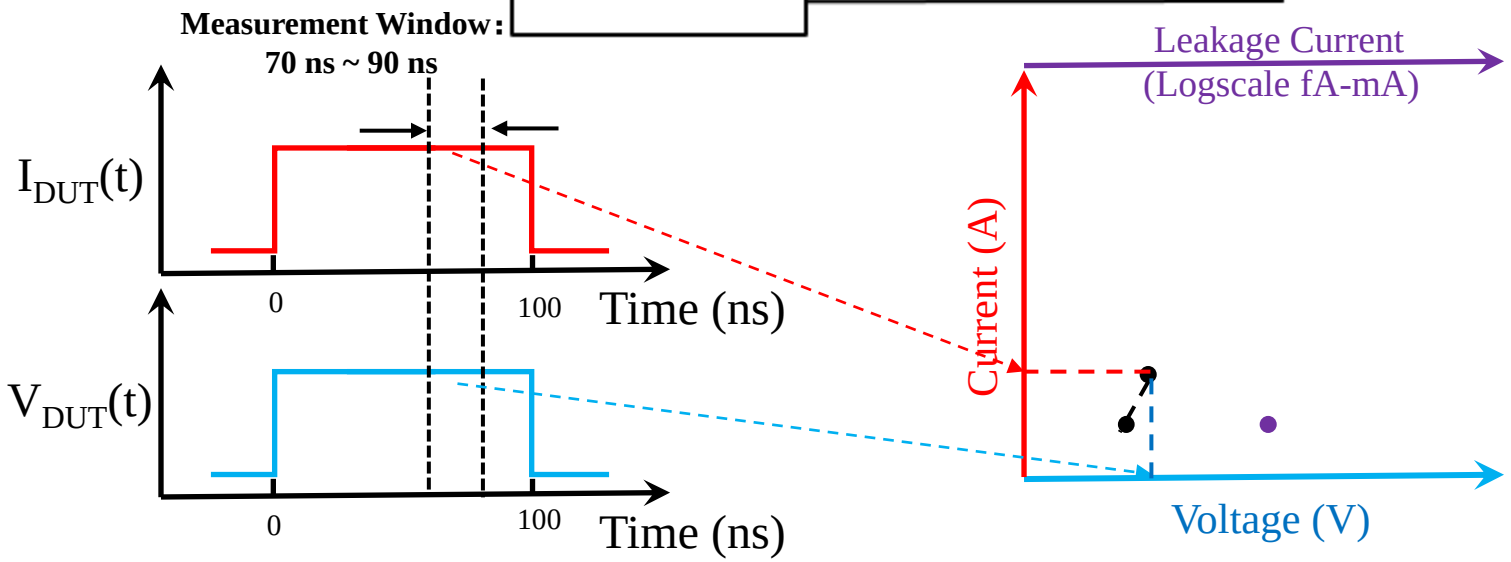
TLP testing IV & Leakage curves obtain

Step 2-A：

Both switches of the Switch Module are set to terminal A. Increase the voltage level of the TLP Pulser, and discharge to the DUT. The oscilloscope capture $I_{DUT}(t)$ and $V_{DUT}(t)$ waveforms, obtain the second pair of (I, V) points.





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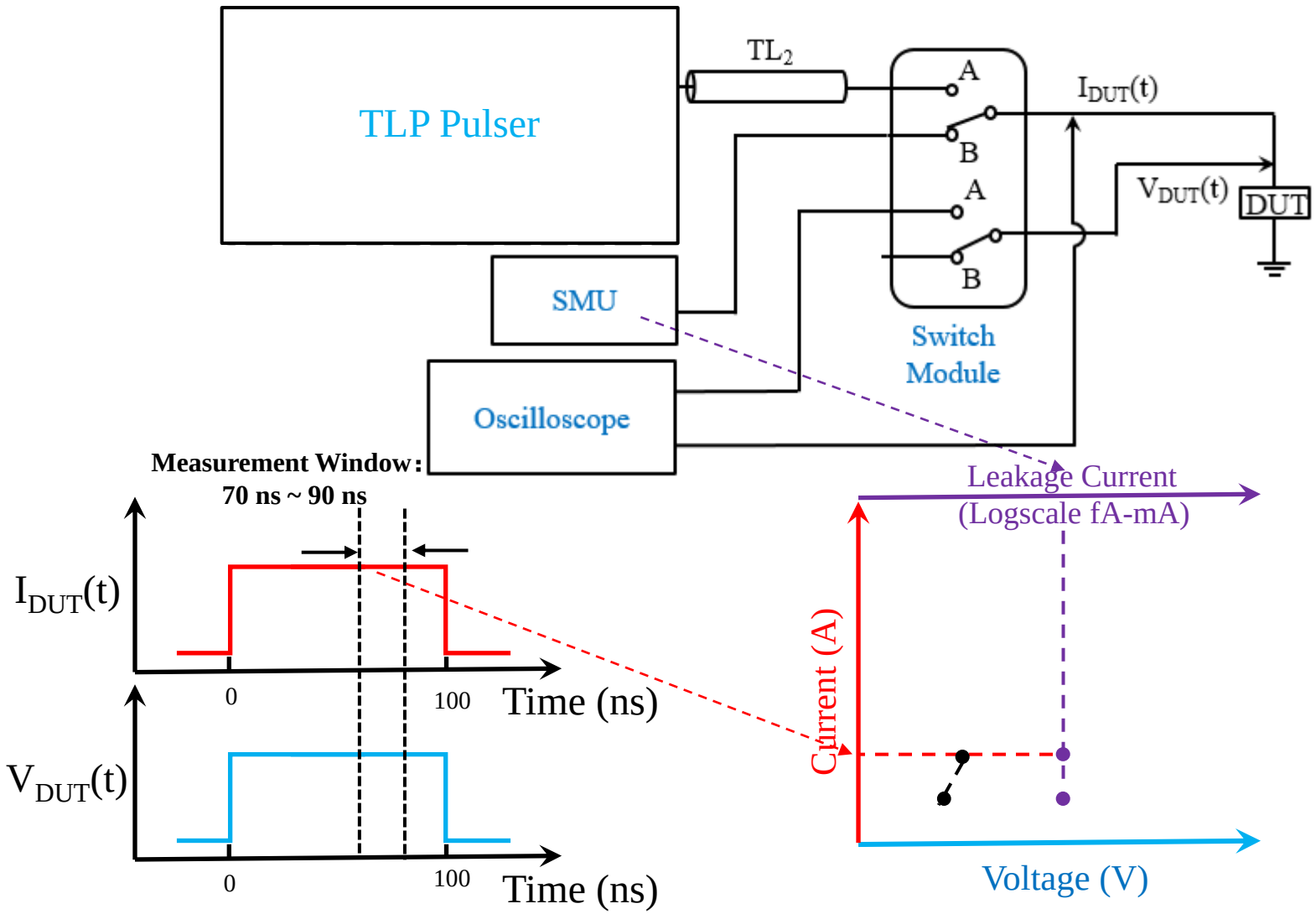
TLP testing IV & Leakage curves obtain

Step 2-B：

Both switches of the Switch Module are set to terminal B, measure leakage current by SMU.



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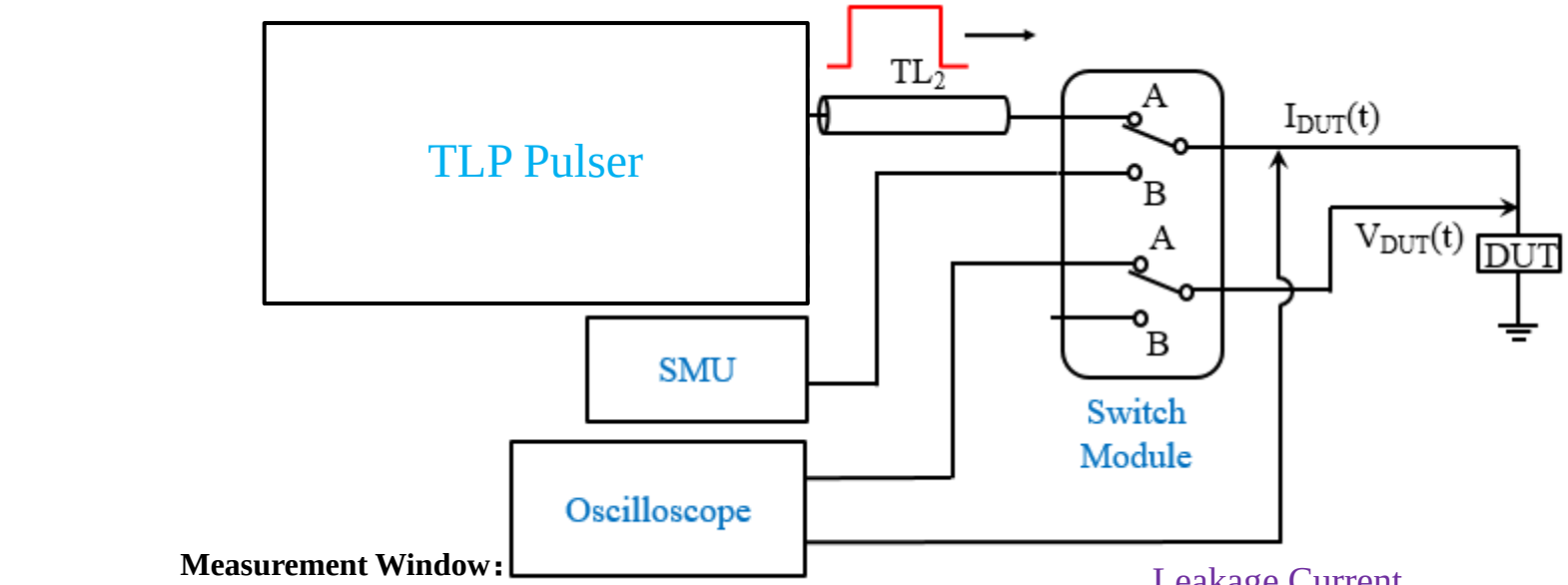
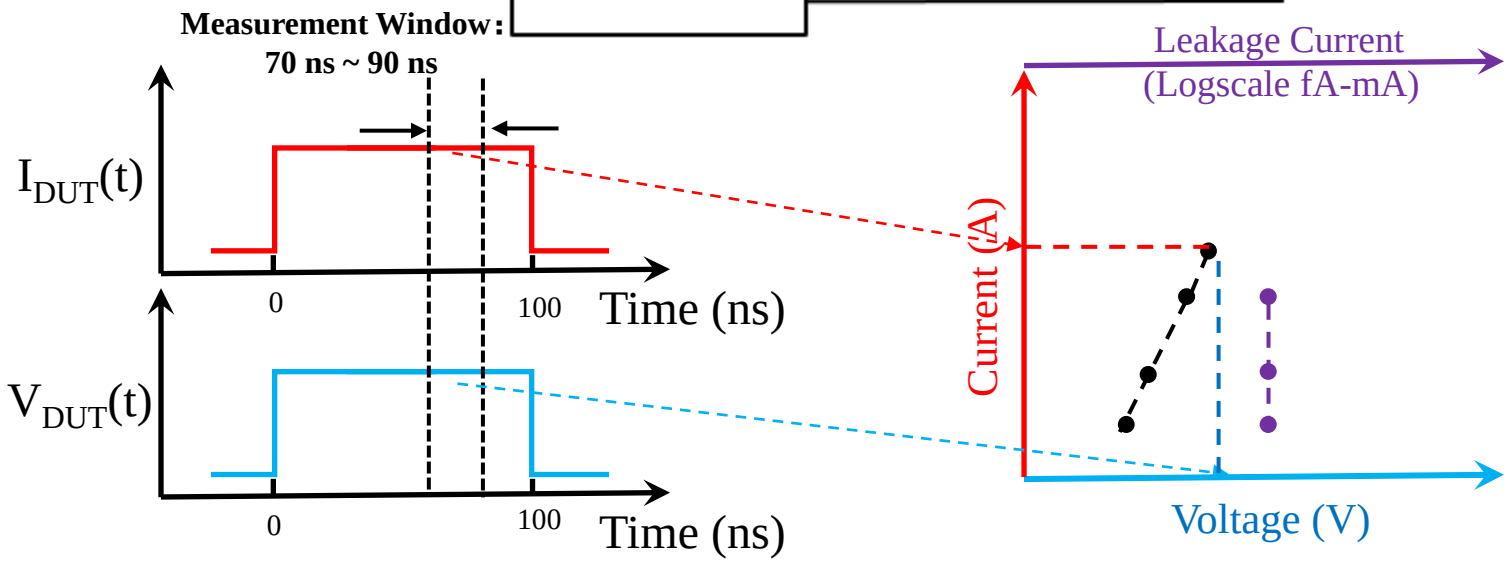
TLP testing IV & Leakage curves obtain

Step N-A：

Both switches of the Switch Module are set to terminal A. Increase the voltage level of the TLP Pulser, and discharge to the DUT. The oscilloscope capture $I_{DUT}(t)$ and $V_{DUT}(t)$ waveforms, obtain the second pair of (I, V) points.





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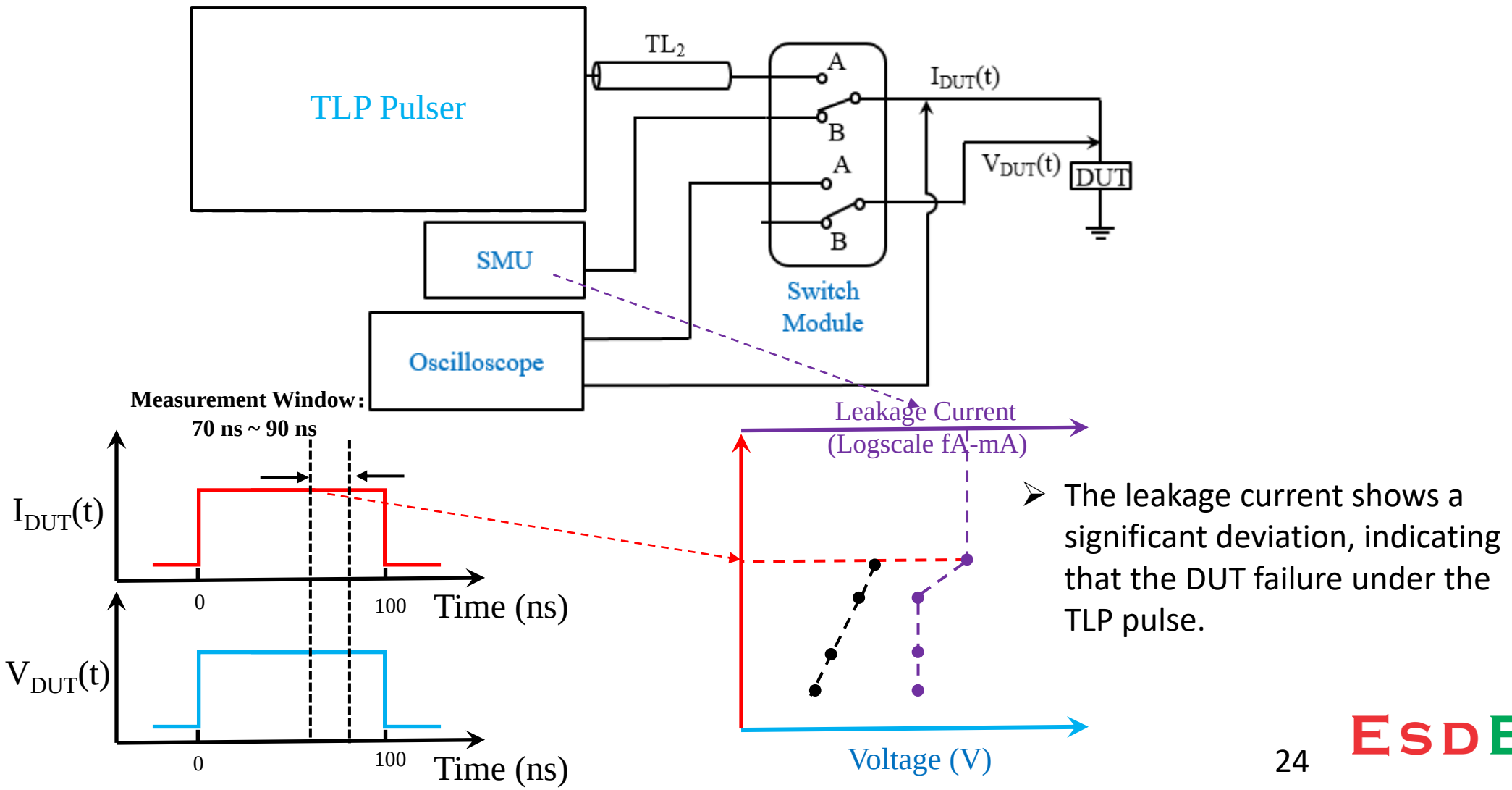
TLP testing IV & Leakage curves obtain

Step N-B：

Both switches of the Switch Module are set to terminal B, measure leakage current by SMU.



- The leakage current shows a significant deviation, indicating that the DUT failure under the TLP pulse.

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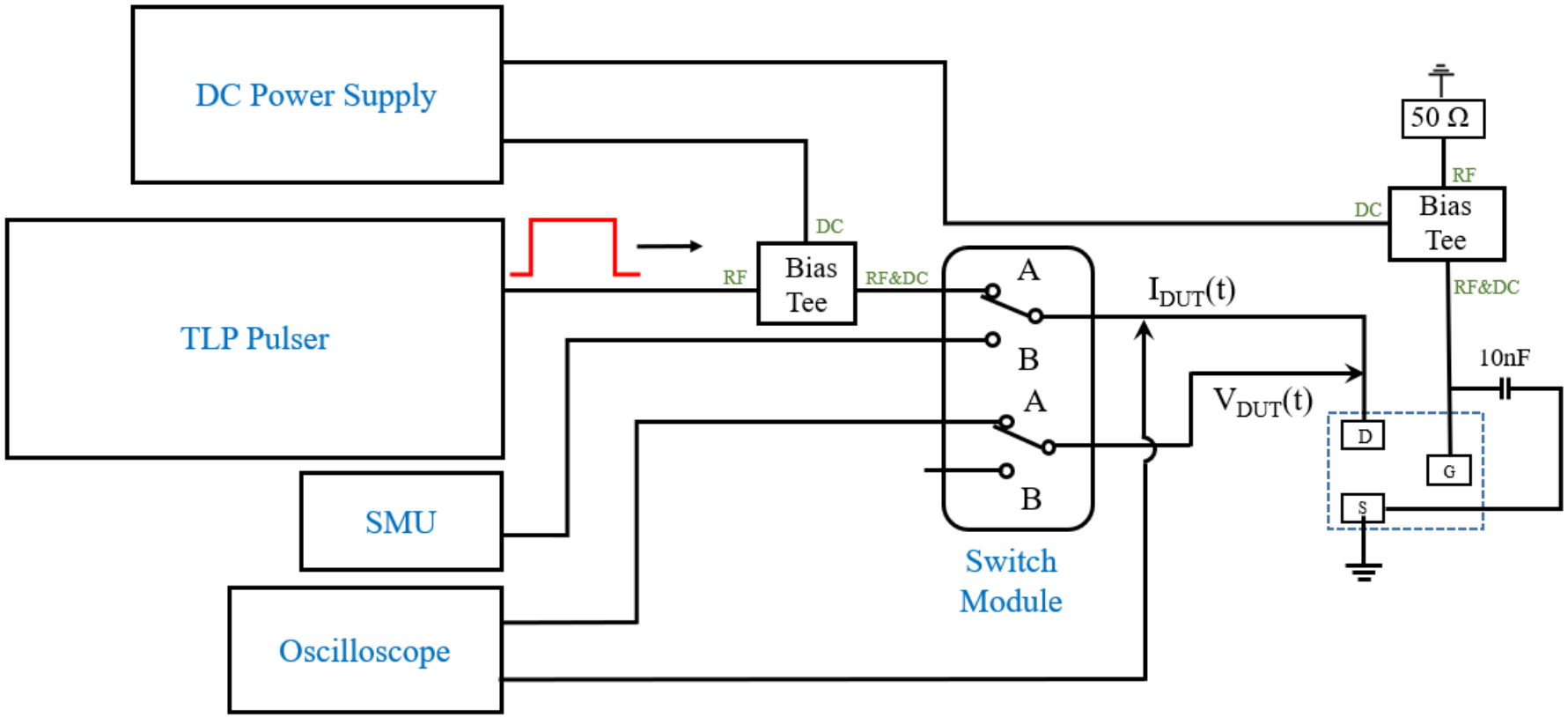
ES622 TLP-SOA testing procedures

Step 1-A：

While the TLP output pulse is generated, a DC source (power supply or SMU) applies a DC bias voltage to the desired pin pair via a Bias Tee.



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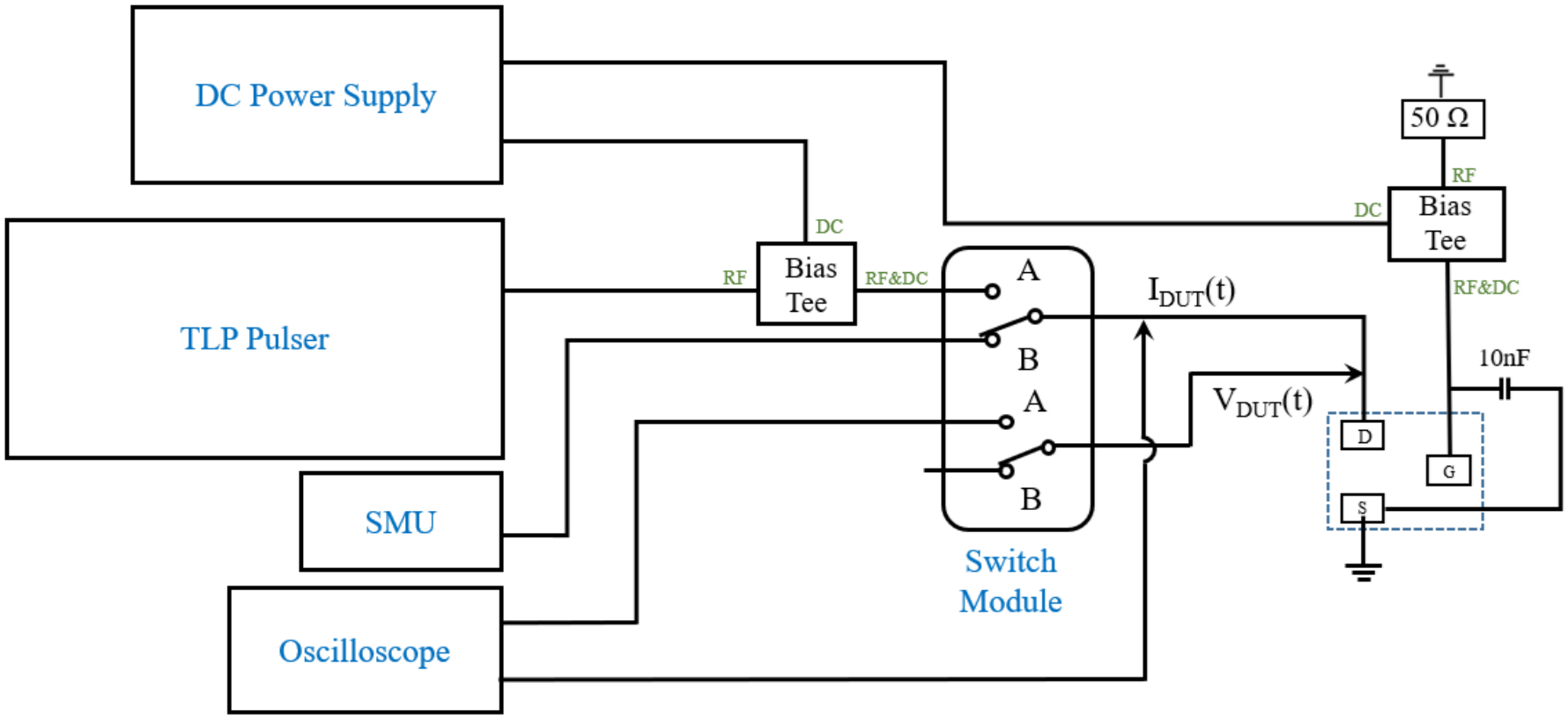
ES622 TLP-SOA testing procedures

Step 2-B：

Both switches of the Switch Module are set to terminal B. The SMU measures the leakage current while DC power supply voltage reduced to 0.



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ESD robustness tests vs. TLP testing

- ESD Robustness of System / IC / Module are often evaluated with different ESD test setups. Some failure types due to transient high energy damage can be simulated with controlled rise-time / pulse-width rectangle TLP pulses or RC circuit discharging into matched 50 Ohm system waveform.
- TLP test results has been used to estimate HBM, IEC 61000-4-2 failure level.
- ESD **thermal failure** correlations*(Note): ***IEC 1 kV level = 2 A , 100 ns TLP pulse level***

  HBM 1.5 - 2 kV level = 1 A, 100 ns TLP pulse level

Notes:

1. Standard TLP doesn't give first peak kind of pulse as IEC 61000-4-2. Device failures caused by the first peak can be repeated by VF-TLP with fast rise-time and short pulse width .
2. Standard TLP test system is usually based on 50 Ohm impedance, while other ESD test systems based on different impedance. The voltage applied before device fully turn-on could be very different and cause different failure types.

Please refer to publications for to TLP test correlations usage, different device has different sensitivities !

[1] *Jon Barth, John Richner. Correlation between transmission-line-pulsing I-V curve and human-body-model.*
[2] *T. Smedes, J. van Zwol, G. de Raad, et al. ESD Relations between system level ESD and (vf-)TLP.*
[3] *YiqunCao, David Johnsson, Bastian Arndt, et al. A TLP-based Human Metal Model ESD-Generator for Device Qualification according to IEC 61000-4-2.*
[4] *Guido Notermans, Peter de Jong and Fred Kuper. Pitfalls when correlating TLP, HBM and MM testing.*
[5] *YiqunCao , Ulrich Glaser , Stephan Freiand, et al.. A Failure Levels Study of Non-Snapback ESD Devices for Automotive Applications.*
[6] *Y. Xi, S. Malobabic, V. Vashchenko, et al. Correlation Between TLP, HMM, and System-Level ESD Pulses for Cu Metallization.*
[7] *Heinrich Wolf, Horst Gieser, KarlheinzBock, et al. Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM.*

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ESD Robustness Tests vs. TLP Testing (Pulse Shape Parameters)

	HBM	MM	IEC (2nd Peak)	IEC (1st Peak)	CDM
Typical max Peak V*	4000V	400V		8kV (contact)	2000V
Typical max Peak I*	< 3A (short)	< 7A (short)	16A (@30ns)	30A	30A
Rise Time*	2 – 10ns	~ns – 10ns	~ns	800ps	< 200ps
Pulse Width*	130 – 170ns	66 – 90ns	~100ns	~5ns	< 400ps
Pulse shape compatible with	Standard TLP	Standard TLP	Standard TLP	VF-TLP	VF-TLP
Typical Failure Modes	Junction damage, metal penetration, melting of metal layers, contact spiking, gate-oxide damage	Junction damage, melting, gate-oxide damage [11]	Melting failure	Oxide punch through	Gate-oxide damage, charge trapping, junction damage

* Typical values noted in each respective standard.

Benefits of TLP testing vs. other ESD tests

- **Well Defined Consistent Waveform Shape**

  Both circuit and waveform defined in ESD simulator standards are too flexible (no impedance control for test path, +-30% tolerance at only certain time spot …) This may lead to different ESD test results among different test sites. TLP pulse is very clean and consistent.

- **Highly Repeatable Test Setup**

  Fatigue from holding ESD simulator with hand leads to inconsistency setup, while TLP test with Jigs for mounting components give a more controlled test.

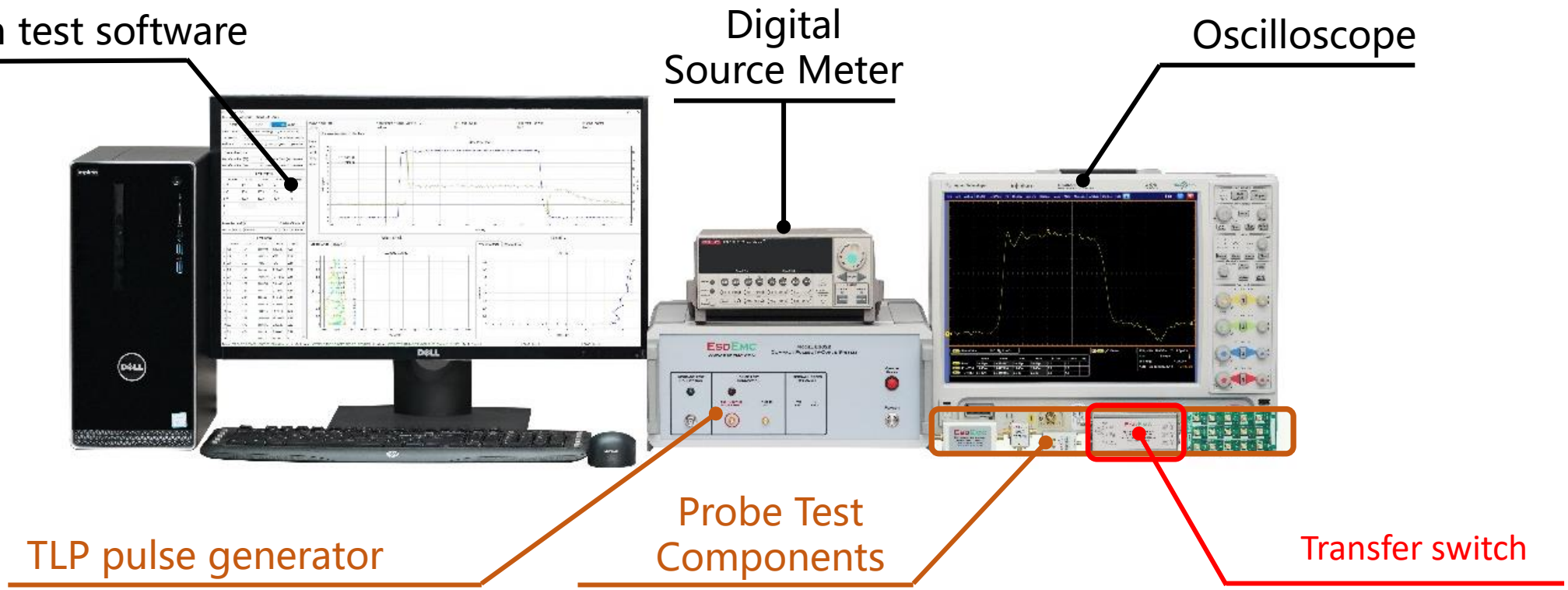
- **Fast Automatic Test, Measurement and Report**

  Usually, TLP test is done with fully automation control of Pulsing, DC Leakage, I-V Curve real-time update and automatic failure detection

- **Important Device Behavior is recorded for ESD analysis and design**

  Many valuable parameters can be extracted from TLP tests for device transient behavior analysis, modeling and System-Efficient ESD Design (SEED). However, traditional ESD tests only generate pulse for P/F results.

ES622 TLP testing system



ES622 test system: Portable Transmission Line Pulse (TLP) IV Curve Test System

Product link:

https://www.esdemc.com/products/device-level-esd-solutions-tlp-vf-tlp-hbm-hmm-eft-surge-mm/es622-series-tlp-pulsed-iv-curve-system-external-modules-available-hmm-hbm-mm/

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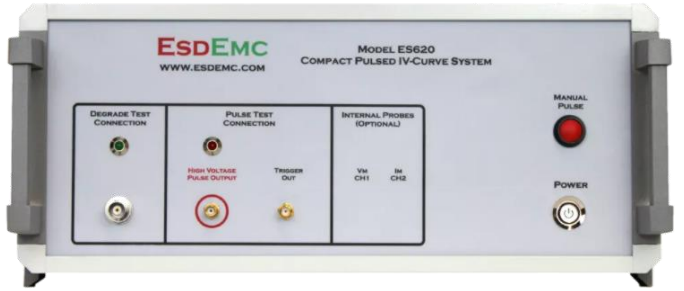
ES622 TLP testing system

1. TLP Pulse Generator (ES62X TLP)
   —— generate and send TLP pulses;



2. Digital source meter (SMU)
   —— Provide DC bias and leakage test;

3. Oscilloscope (OSC)
   ——Collect the transient voltage and current waveforms at the;

4. Transfer switch (SW)
   ——Realize mode switching between TLP test and leakage test;

5. Voltage and current measurement fixture
   ——Capture the transient voltage and current at the

6. Computer (PC)
   ——Realize the intelligent control of the whole system, and automatically record and analyze the test results.

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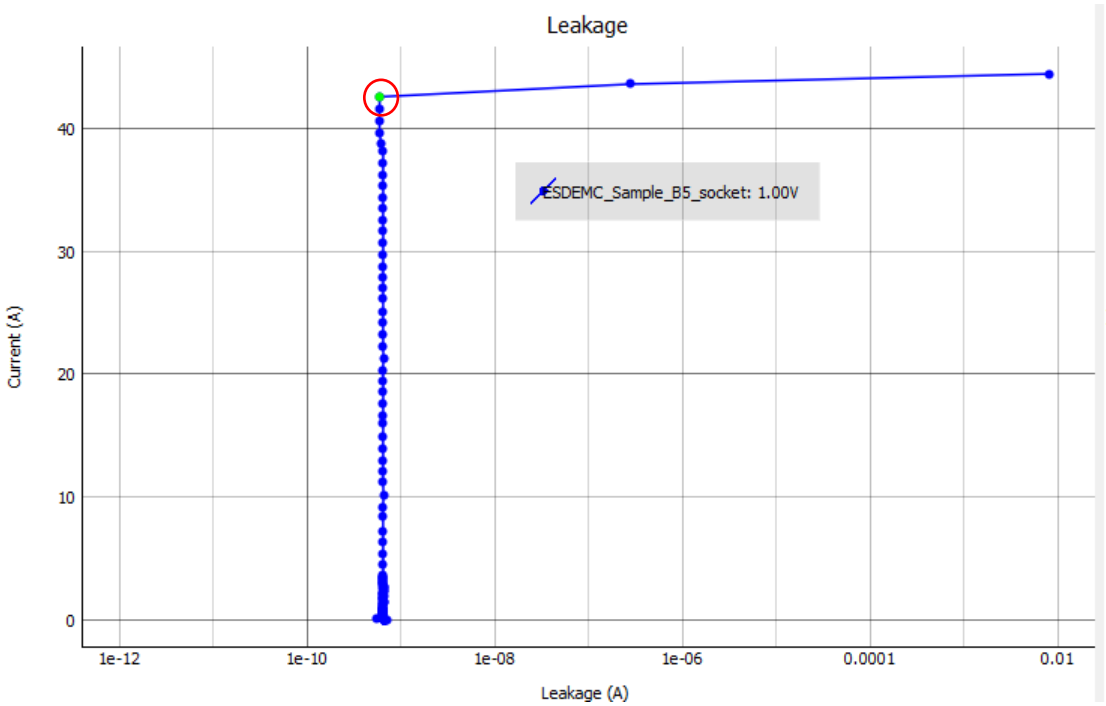
ES622 TLP system general testing procedures

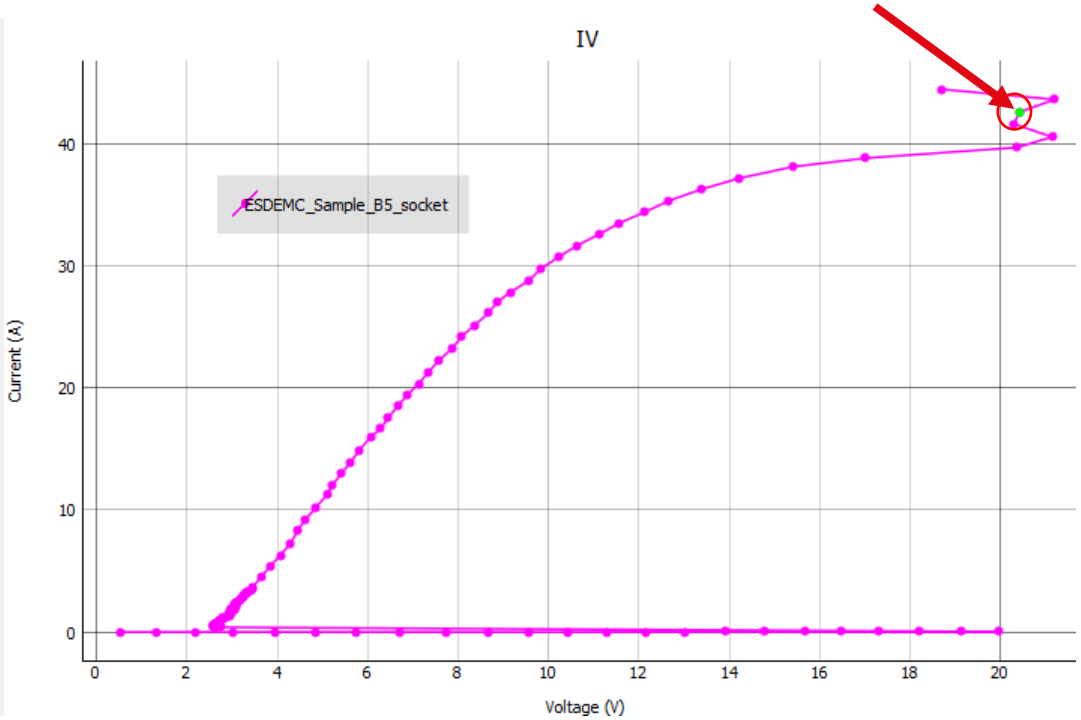
- Timing
  - Measure a device (better a resistor) to calibrate voltage and current waveform starting point
- SOZL (Short – Open – Zener – Load) Calibration
  - Short and Open measurements provide Series and Shunt resistances, respectively
  - Zener and Load measurements provide Voltage and Current correction factors, respectively
  - This calibration should be performed every few months or if equipment is changed
- Calibration verification
  - Measure a well-known device
- Testing

TLP testing Applications

1. Measure DUT pulsed **I-V curve** and **leakage** curve.



Failure level: 42.57A



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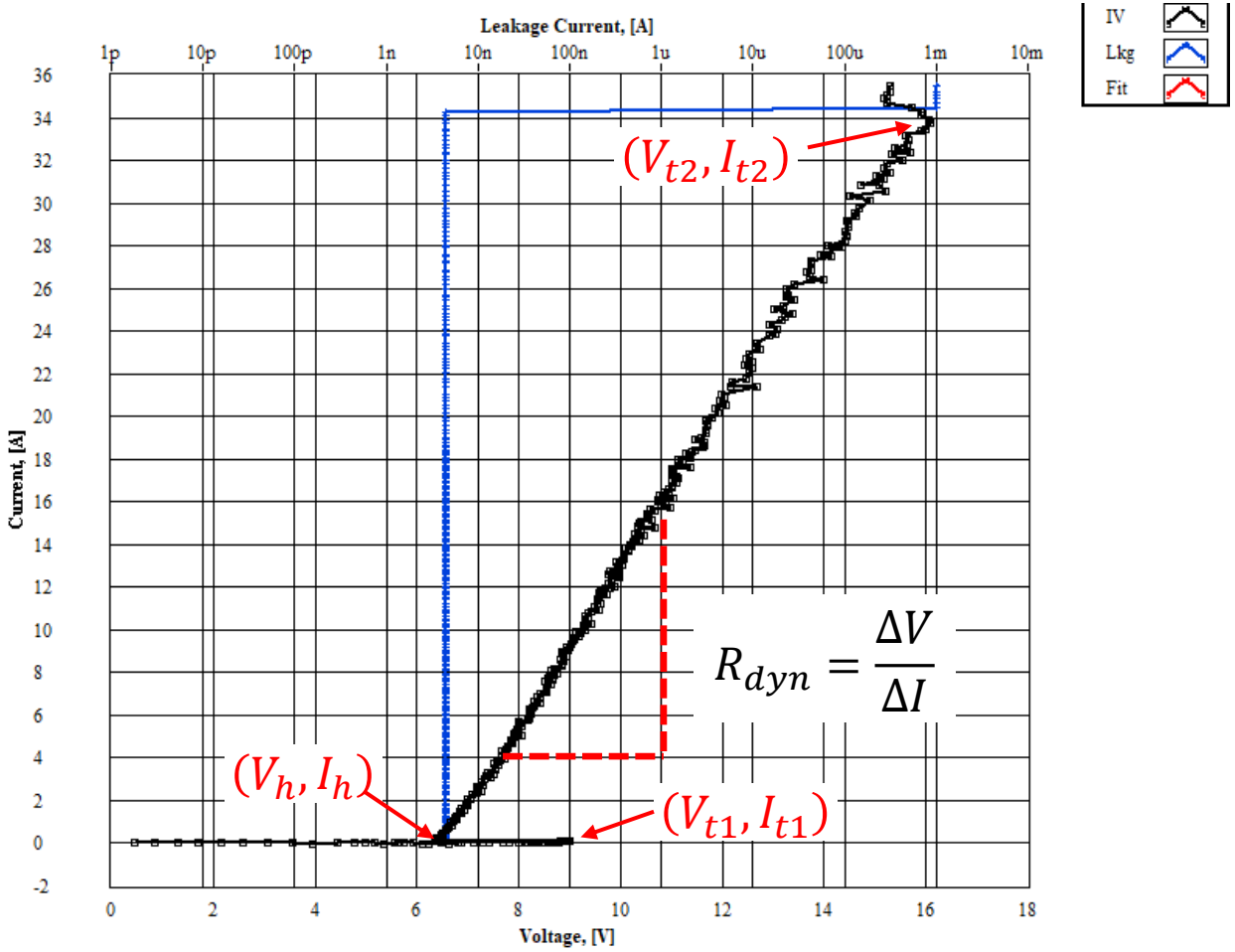
TLP testing Applications

2. Characterize device: **turn on** point, **snapback** point, **failure** level, **dynamic Resistance** R_{dyn}.



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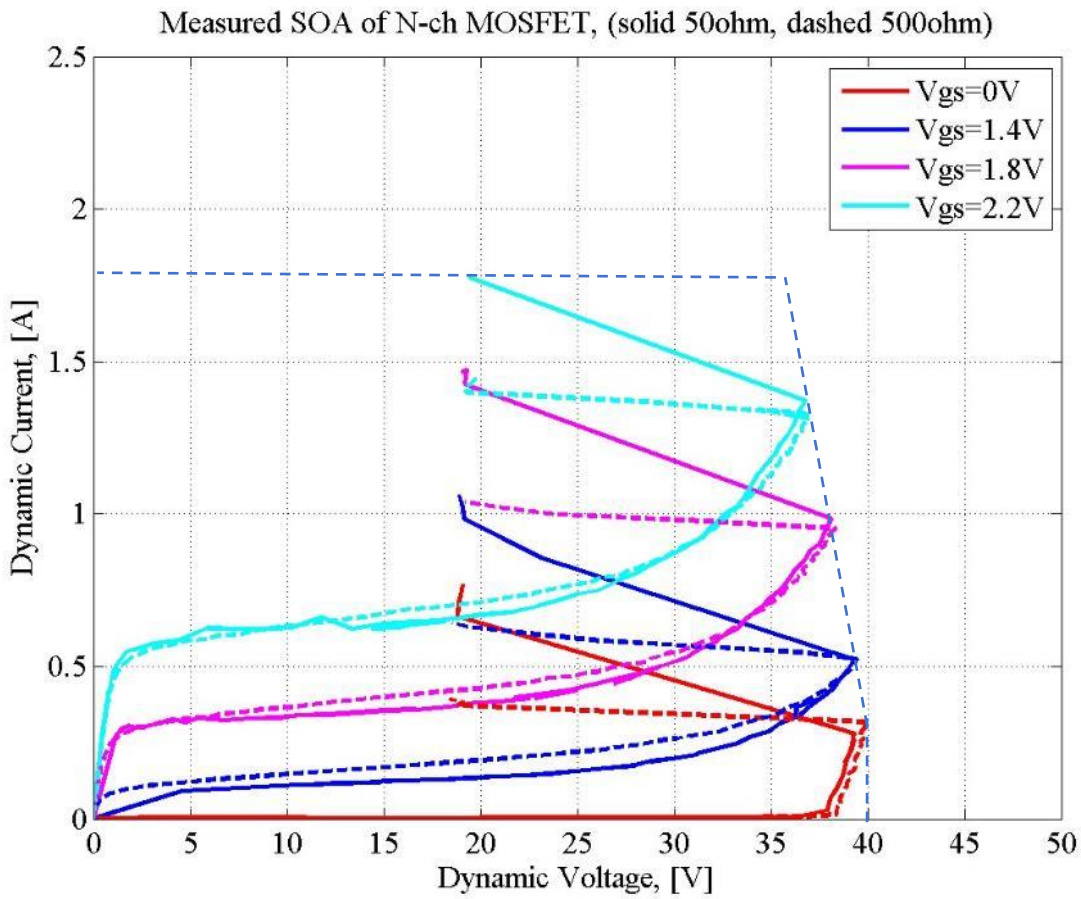
TLP testing Applications

3. Obtain MOSFET pulsed **Safe Operating Area** (SOA).



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TLP testing Applications

4. VF-TLP application: device **turn on time**.

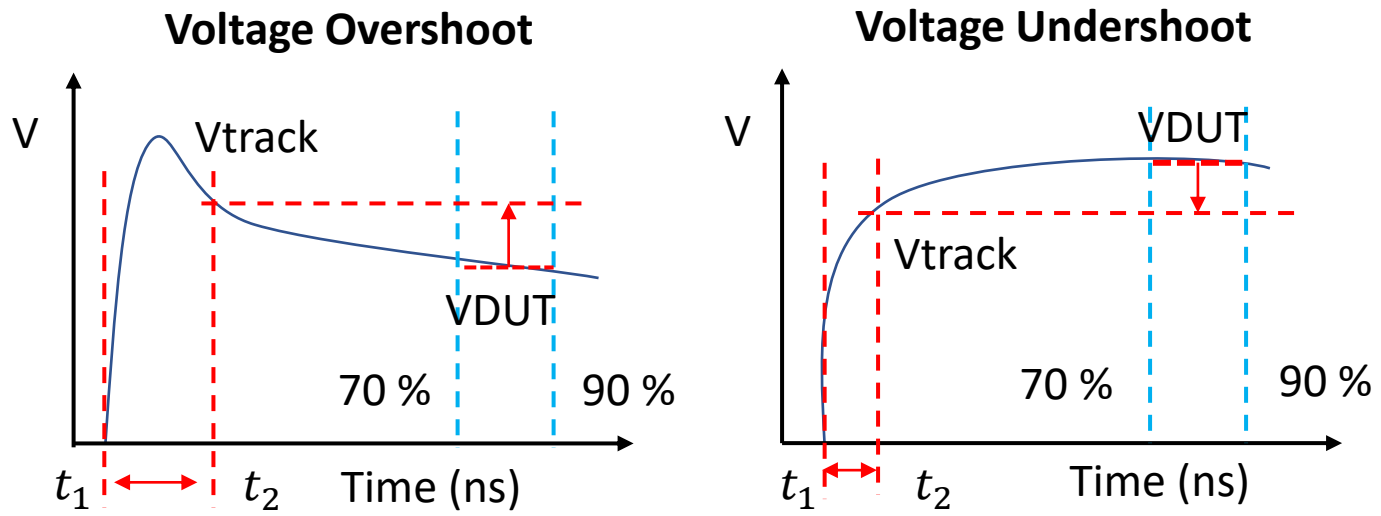
Vertical blue lines: 70 % to 90 % TLP average window

- VDUT = mean(V[70%:90%])

Horizontal red line: VDUT ± 30%

- Used to calculate the turn-on time

$$T_{turn\_on} = t_2 - t_1$$



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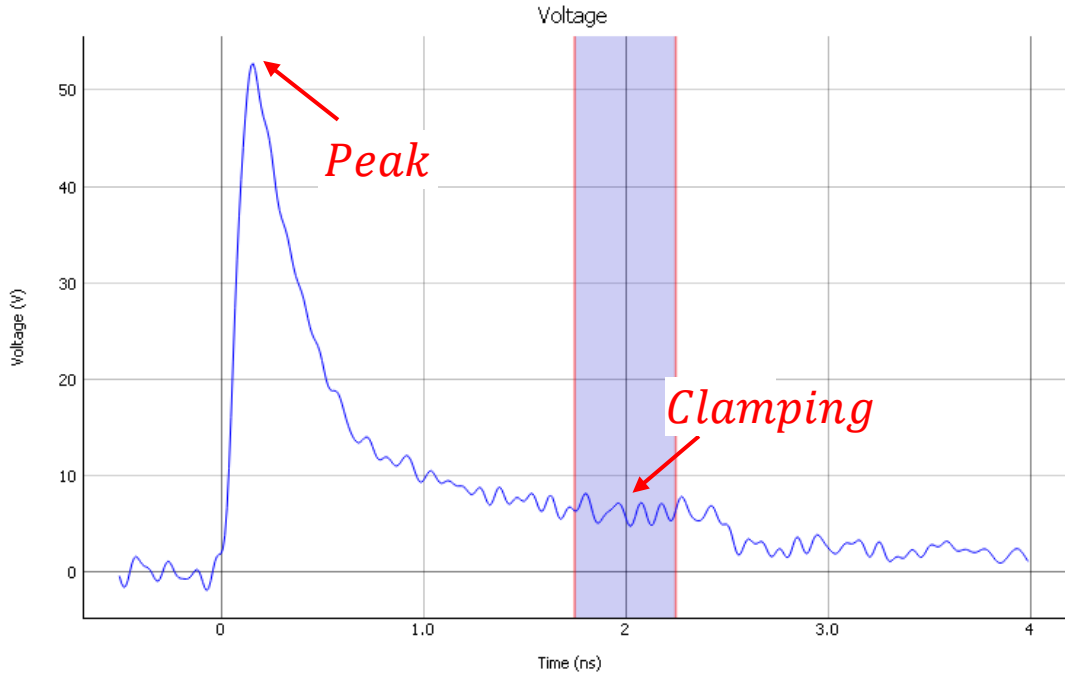
TLP testing Applications

5. VF-TLP application: device **peak & clamping voltage**.

Some devices are sensitive to peak voltage (high E-field strength), therefore both parameters are important to understand the device sensitivity and design best ESD protection solution.



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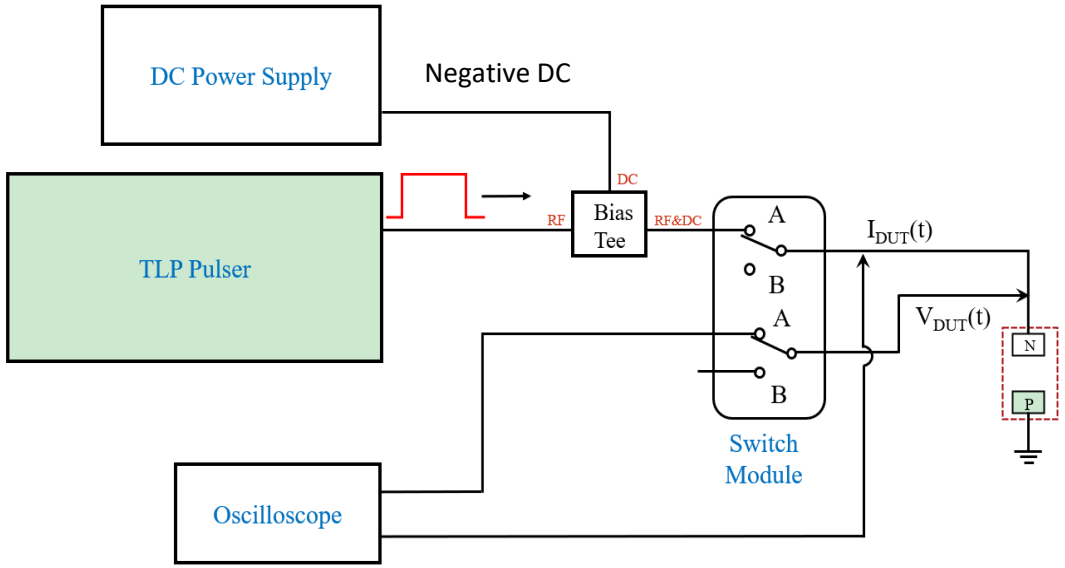
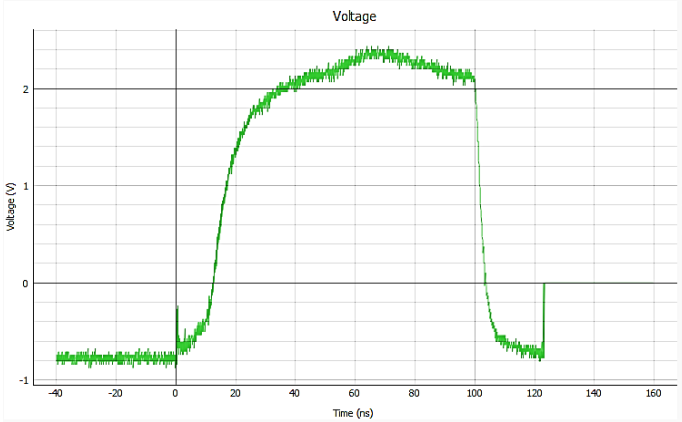
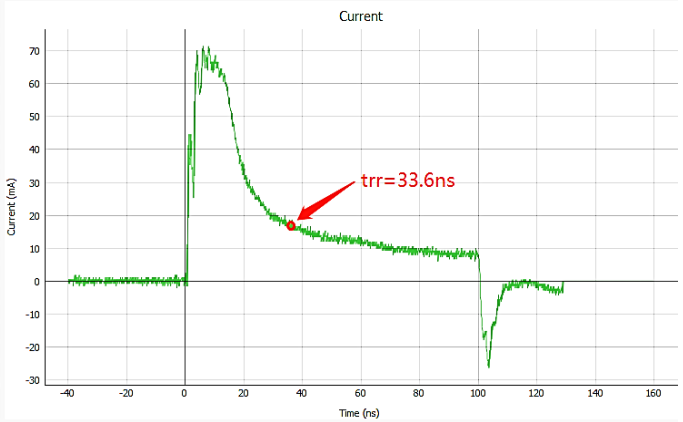
TLP testing Applications

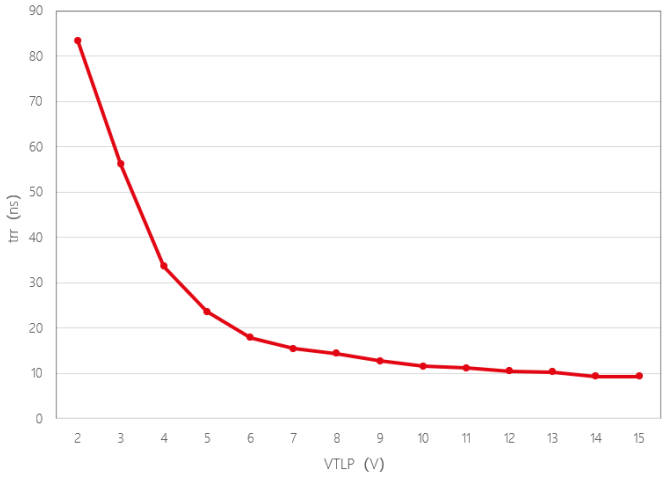
6. Characterize device Charge recovery effects

- Reverse recovery time: The time interval during which the current transitions from forward direction to reverse direction and then decreases from the maximum reverse value to a specified value (typically 25% of the maximum reverse current).









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TLP testing Applications

7. Characterize device linearity under pulsed transient
   e.g. capacitance changes over high voltage

8. Characterize device break down effects
   e.g. Touch panel sensor traces sparking / fuse effect during ESD

9. Characterize saturation effects on common mode chokes and Ethernet magnetics

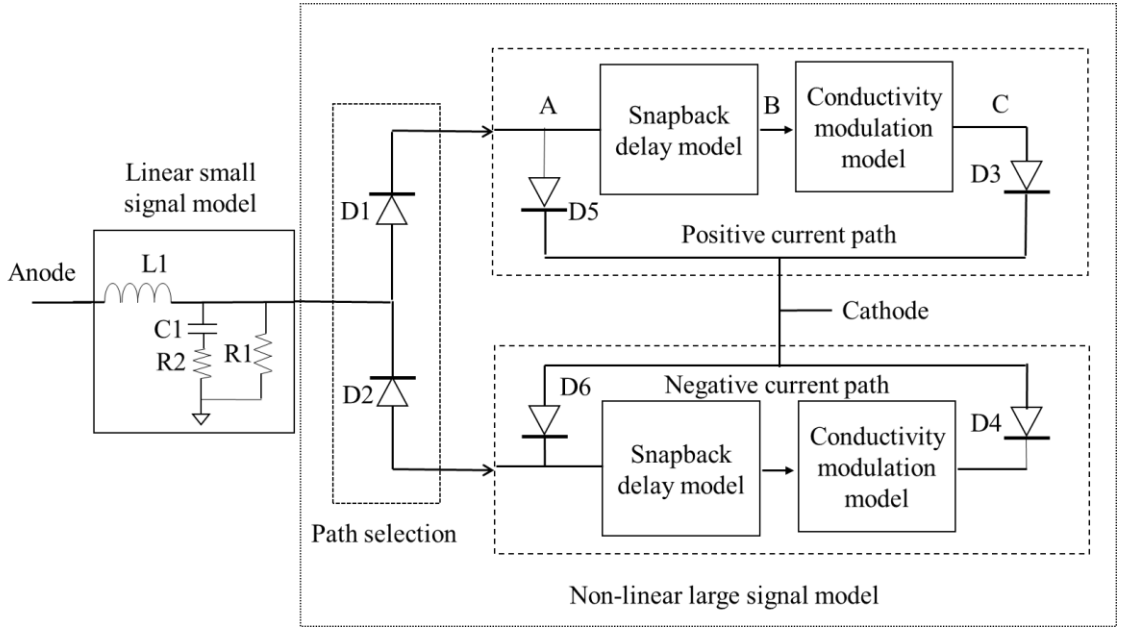
10. Measure the non-linearity of capacitance of Multi-Layer capacitors

TLP testing Applications

For system level, TLP tested results could be:

1. Guidelines for component selection. For example:
   - ESD protection device turn on & hold voltage should higher than IC pin operating voltage, lower dynamic resistance, and higher failure level;
   - Choose the components with fast turn on time and low overshoot;

2. Large signal parameters for SEED modeling[1]



[1] *P. Wei, G. Maghlakelidze, A. Patnaik, H. Gossner, and D. Pommerenke, TVS Transient Behavior Characterization and SPICE-Based Behavior Model.*

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TLP System Configuration Considerations

TLP system configuration depends on the required applications.

1) TLP generator specification:

- **Rise time**: 0.1 or 0.2ns (*match CDM*), 1ns (*match HMM*), 2 ~ 10ns (*match HBM*) Can select multiple values

- **Pulse width**: 1 ~ 10ns (*VF-TLP*)
  100ns (*standard TLP*)
  500ns or longer (*large energy injection*) Can select multiple values

- **Maximum current/voltage level**: 25A/1.25kV (*IC testing*)
  50A/ 2.5kV (*can cover most TLP applications*)
  100A/ 5kV or higher (*ESD protection devices*)

- **Pulse shape**: TLP (rectangular waveform), HBM, HMM Can select multiple modules

For more TLP specification, please refer to:

https://www.esdemc.com/products/esd-tlp-systems-tlp-vf-tlp-hbm-hmm-eft-surge/es620-pulsed-iv-curve-analysis-system/

https://www.esdemc.com/products/esd-tlp-systems-tlp-vf-tlp-hbm-hmm-eft-surge/es622-series-tlp-pulsed-iv-curve-system-external-modules-available-hmm-hbm-mm/

TLP System Configuration Considerations

2) **Oscilloscope specification:**Bandwidth & sampling rate

- **Standard TLP testing system** needed bandwidth depends on the IV measurement window. Most standard TLP testing applies 100 ns pulse width, and the IV window is 70ns - 90ns (70%- 90% pulse width). In this situation, **200 MHz bandwidth** is sufficient to measure IV curve.

- VF-TLP testing system needed bandwidth depends on the pulse rise time, because the DUT first several nanoseconds' behaviors wanted to be captured. In is situation, the recommended oscilloscope bandwidth will be 4 ~ 8 GHz, and the voltage probe bandwidth shall not be below 3 times the single shot bandwidth of the applied oscilloscope.

Pulse Width / Rise Time	Single Shot Bandwidth	Sampling Rate
≥100 ns / ≥10 ns	100 MHz	0.5 Gsample/s
10 ns / 1 ns	1 GHz	3 Gsample/s
5 ns / 0.5 ns	2 GHz	6 Gsample/s
1 ns / 0.1 ns	6 GHz	20 Gsample/s

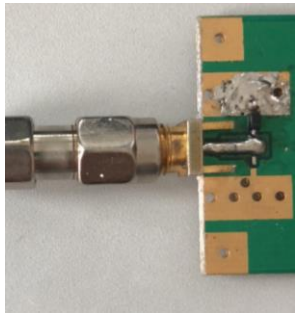
TLP System Configuration Considerations

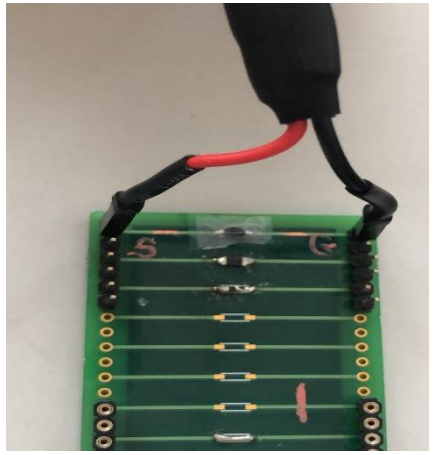
3) DC and Bias Measurement:

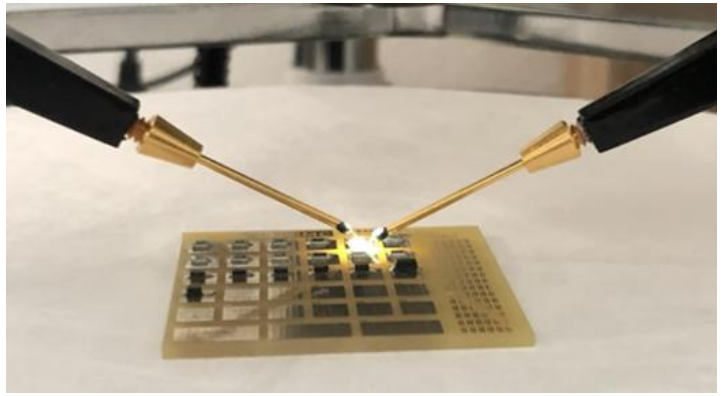
- **SMU** (for DC IV curve & leakage testing) & **DC Power supply** (for SOA or power-on TLP testing) maximum voltage depends on DUT max operating voltage

4) Testing fixture:

- PCB with SMA connector
- Socket/hook
- Probing with probe station







TLP System Specification on Market

- Standard TLP System
  - Common spec: **2 kV open voltage / 40A short current**
    - ESDEMC Standard TLP Solution currently can provides up to **7.5kV / 150A**, the highest pulse injection and IV measurement specification in the world)
    - Nearest competitors: **6kV / 120A, Others 2kV / 40A**

- VF-TLP System
  - Common spec: Injection level up to **1kV / 20A**, with clean, fast and stable rise-time (<100 ps), wide analogue measurement bandwidth and advanced digital frequency compensation
    - ESDEMC VF-TLP Solution currently can provides
      - TLP Pulse up to **1kV / 20A with 60 ps rise-time** and up to 2.**5 kV / 50 A with 200 ps rise-time**
      - Measurement with up to 6 GHz analogue bandwidth measurement capability plus all port frequency compensation algorithm using Network Analyzer S-parameters

World's Top Specification TLP Dynamic IV-Curve Solution

Specifications/Functions	ESDEMC ES620/ES622	Other Brand Systems
Fastest Rise-time	~ 50 ps (2021 spec)	100 ps, 200 ps
Longest Pulse-width	2000 ns TLP (1ms EOS)	1600 ns, 400 ns
Maximum Current Injection Level	150 A	120 A, 40A, 30A…
Standard 2D IV Curve Analysis	Yes	Yes
Advanced 3D IVT Curve Analysis	Yes, currently unique	No, need additional work
Voltage Measurement Methods	Resistive Direct, Overlap TDR, Non Overlap TDR,	Usually only 1 or 2 types
Current Measurement Methods	Resistive Direct, Resistive Equation, Inductive Direct, Overlap TDR, Non Overlap TDR	Usually only 1 or 2 types
Error Correction Methods	SOLZ Correction, All ports S-parameters compensation, Trigger timing alignment	SOLZ Correction
Differential TLP Pulsing and IV Test	Yes, unique	No

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Thank you !

- Please feel free to contact info@esdemc.com for questions about general ESD test and applications, we are expert in this field and we like to help !

- We will keep updating this ppt and we offer FREE application consulting. We also send out latest technical notes and sales promotion each quarter, please email us if you like to subscribe.

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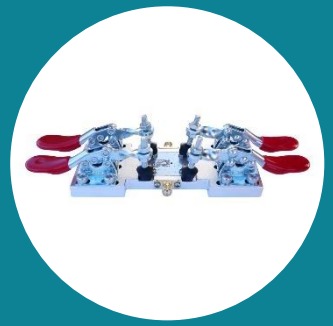
ESD Test Solution

EMC Test Solution

High Voltage System Design

High Frequency System Design



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Graph 3: Reference 10