Characterization of TVS Diodes for ESD Protection Applications

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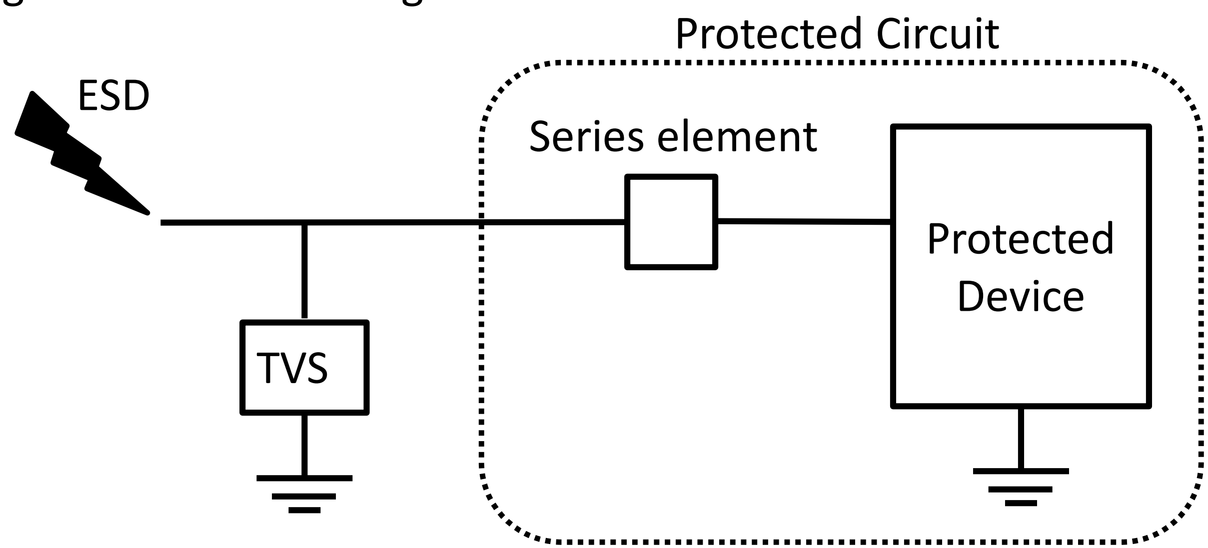
TVS operation principle

- TVS devices are designed to protect sensitive electronics from the damaging effects of electrostatic discharge (ESD). They are NOT useful to prevent EOS damage as they excel at handling large currents for short times (30 A for 50 ns) but cannot handle long stress currents (100 mA for 100 ms) due to their low thermal capacity.
- During normal operating conditions, TVS devices appear to be an open circuit (with small leakage current). Under stress conditions, these devices turn on, providing a low impedance path to the transient current. The voltage across the protected circuit is restricted to the clamp voltage of the TVS diode.
- The ESD protection device is placed before the desired component/circuit to be protected from ESD damage as shown in the figure below.

Typical ESD protection device implementation.

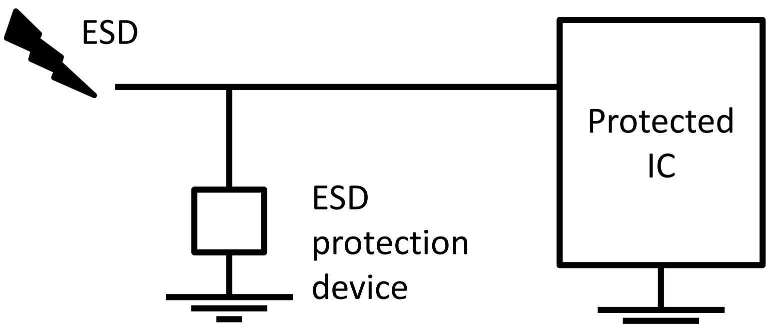
A series element may or may not be included, in the protected device path.



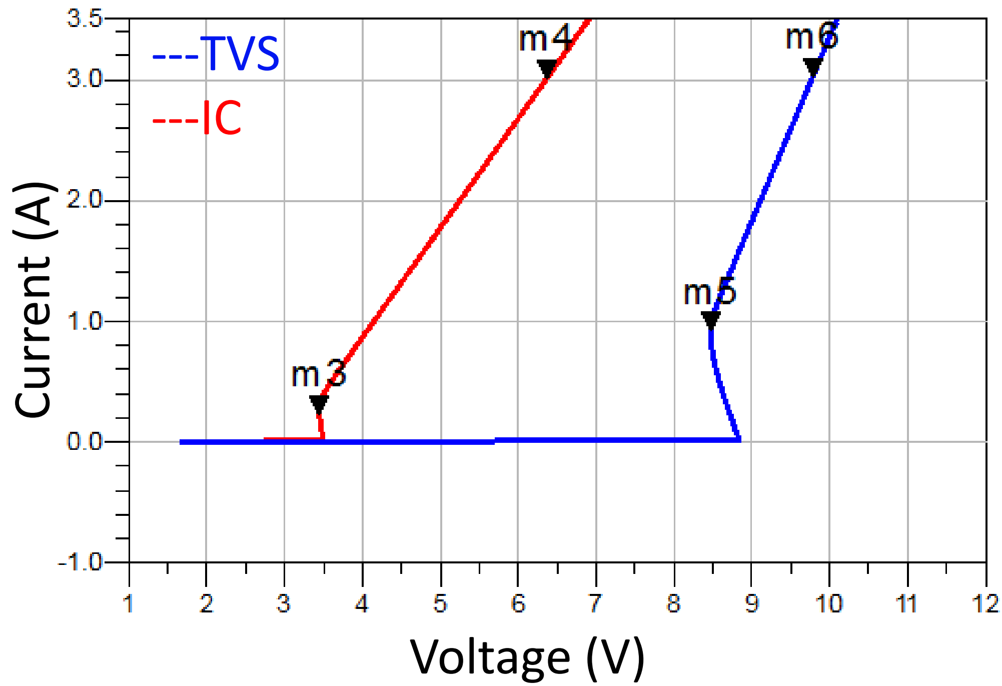
Quasi-static IV curve

By comparing the quasi-static *IV* curve of the IC and TVS device, it is observed that the TVS device turns on at a higher voltage. However, it can be shown that for short pulses in the 1-2 ns range, the TVS diode is capable of protecting the IC in spite of the higher turn-on voltage revealed by the *IV* curve.

Block diagram of the IC pin with TVS diode setup



I-V curve



How to characterize a TVS

- At present, TVS diode manufacturers characterize their devices using different test setups, only capturing a subset of the relevant parameters

- Datasheets place an emphasis on favorable parameters
  - As a result, TVS diodes are hard to compare based on manufacturers data

- Characterize various 0201 package TVS diodes from different vendors through:

1. VF-TLP characteristics:

(a) Transient waveforms; (b) IV curve & Turn on time; (c) Turn on voltage;
(d) Dynamic resistance; (e) Clamping voltage; (f) Failure threshold

2. Effect on signal integrity

(a) Capacitance; (b) package inductance; (c) Insertion loss;

3. ESD generator contact mode behavior

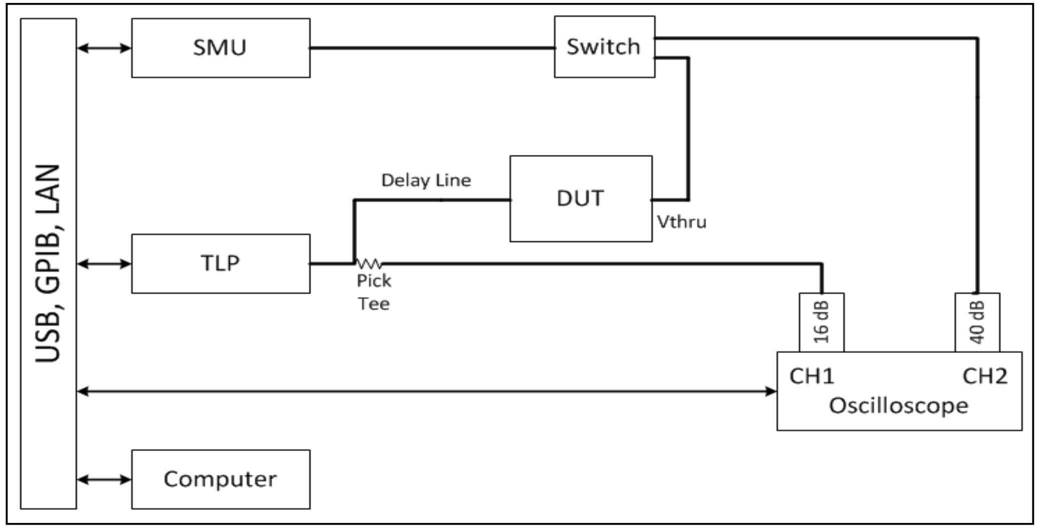
VF-TLP Test setup

Oscilloscope:

- Teledyne Lecroy, 20 GSa/s, 6 GHz

SMU:

- Leakage Polarity = Positive
- NO. of points = 1
- Test DC Value = 1 V



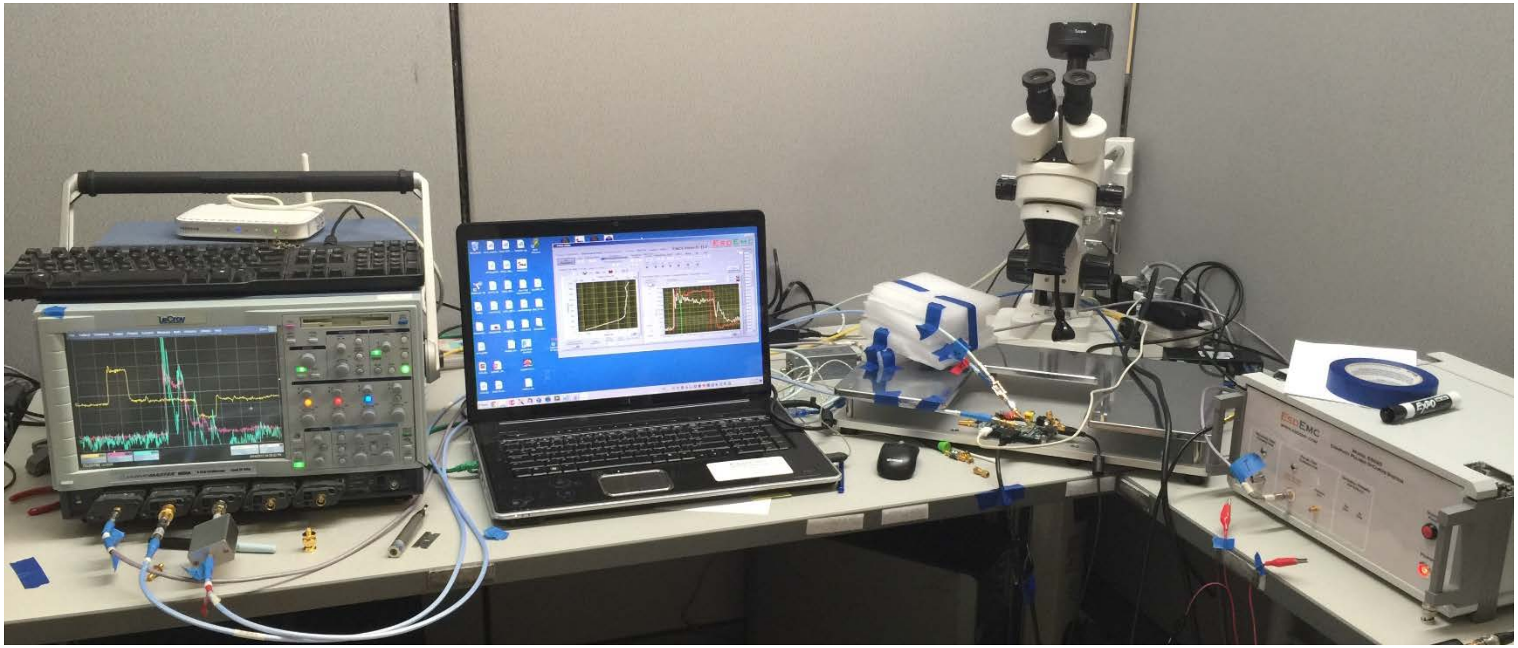
VF-TLP test setup

VF-TLP Test Fixture

VF-TLP:

- ESDEMC ES620-50 VF-TLP system
- Pulse width = 6 ns
- Rise time of the pulse = < 250 ps
- Max TLP pulse voltage = ~ 2.5 KV
- Measurement window: 70 % to 90 % of the 6 ns pulse width (4.2 ns to 5.4 ns).
- TLP Polarity = Both polarities of the diodes are tested.
- voltage pulse range: 0.7 V to 40 V (no. of points = 40) & 40 V to 1.9 KV (no. of points = 94)
- The TLP is a 50 Ω system, whereas the ESD gun can be seen as a 270 Ω system. An 8 KV ESD Gun will generate similar current levels to a 1.5 KV TLP.
- S-parameters of all the cables & attenuators used in the VF-TLP test setup are measured and corrected for the losses introduced by them in the system.

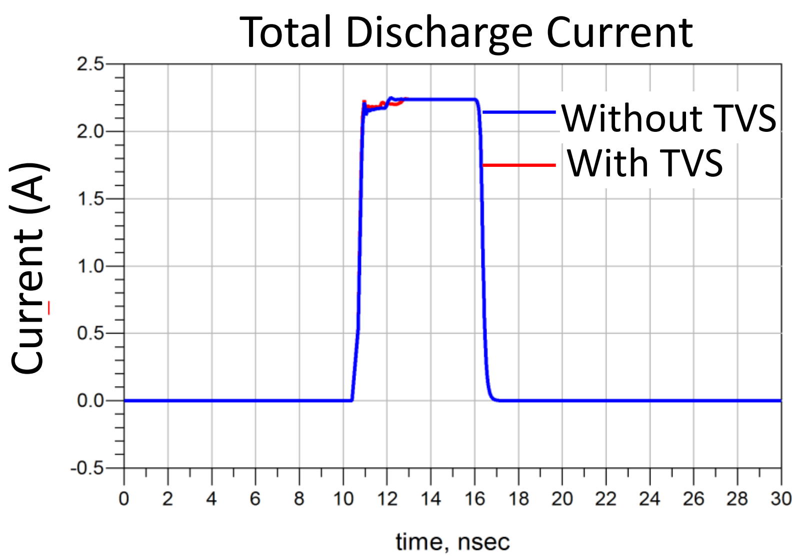
VF-TLP IV- Curve Test System

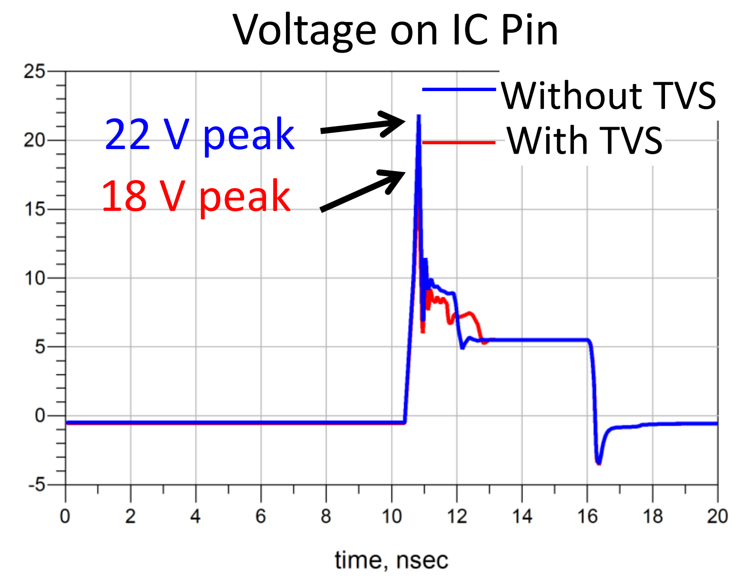


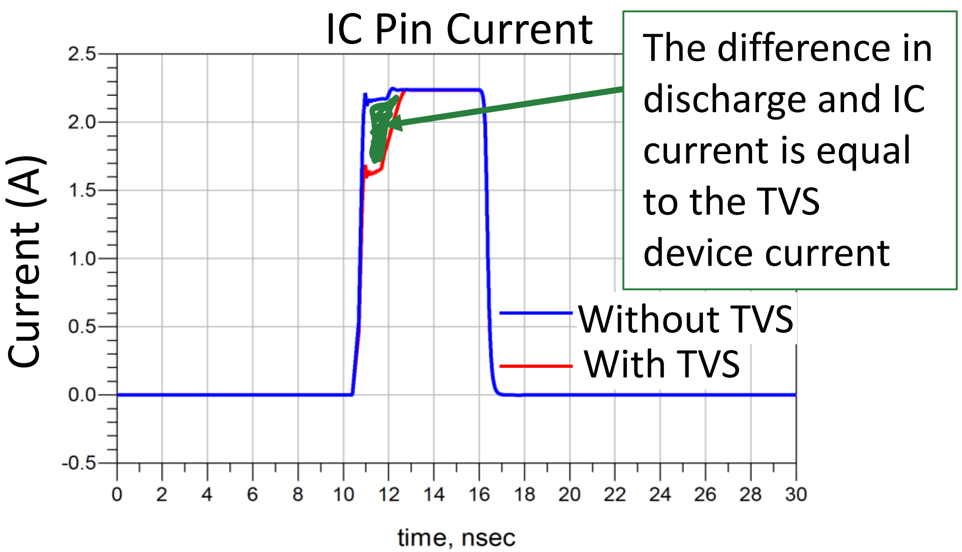
Product link:
ES620-50 VF-TLP system:
https://www.esdemc.com/products/esd-tlp-systems-tlp-vf-tlp-hbm-hmm-eft-surge/es620-pulsed-iv-curve-analysis-system/

VF-TLP Transient Waveforms

Here an IC pin is compared to a TVS device in terms of TLP transient waveforms.







Because the TVS device carries some current in the first nanoseconds of the pulse, this limits the peak voltage seen at the IC. In this case, an improvement of 4 V is seen.

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VF-TLP: Defining IV Curve & Turn-on Time

Vertical blue lines: 70 % to 90 % TLP average window

- VDUT = mean(V[70%:90%])

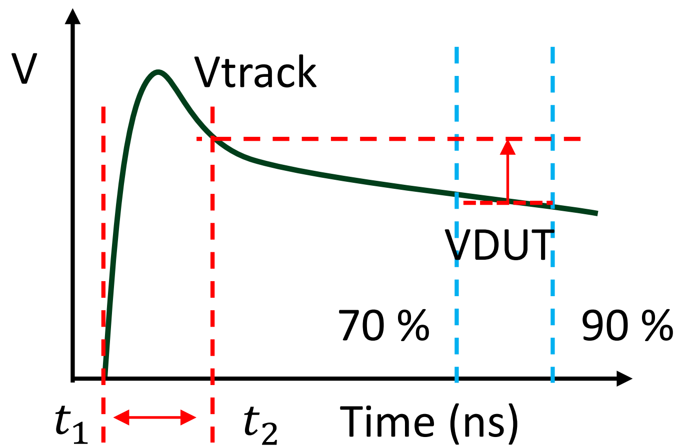
Horizontal red line: VDUT ± 30%

- Used to calculate the turn-on time

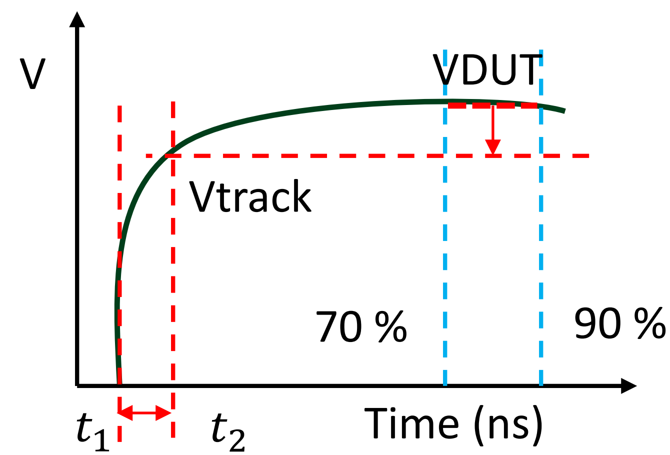
Vertical red lines: t_1 and t_2 used to calculate the turn-on time

$$T_{turn\_on} = t_2 - t_1$$

Voltage Overshoot



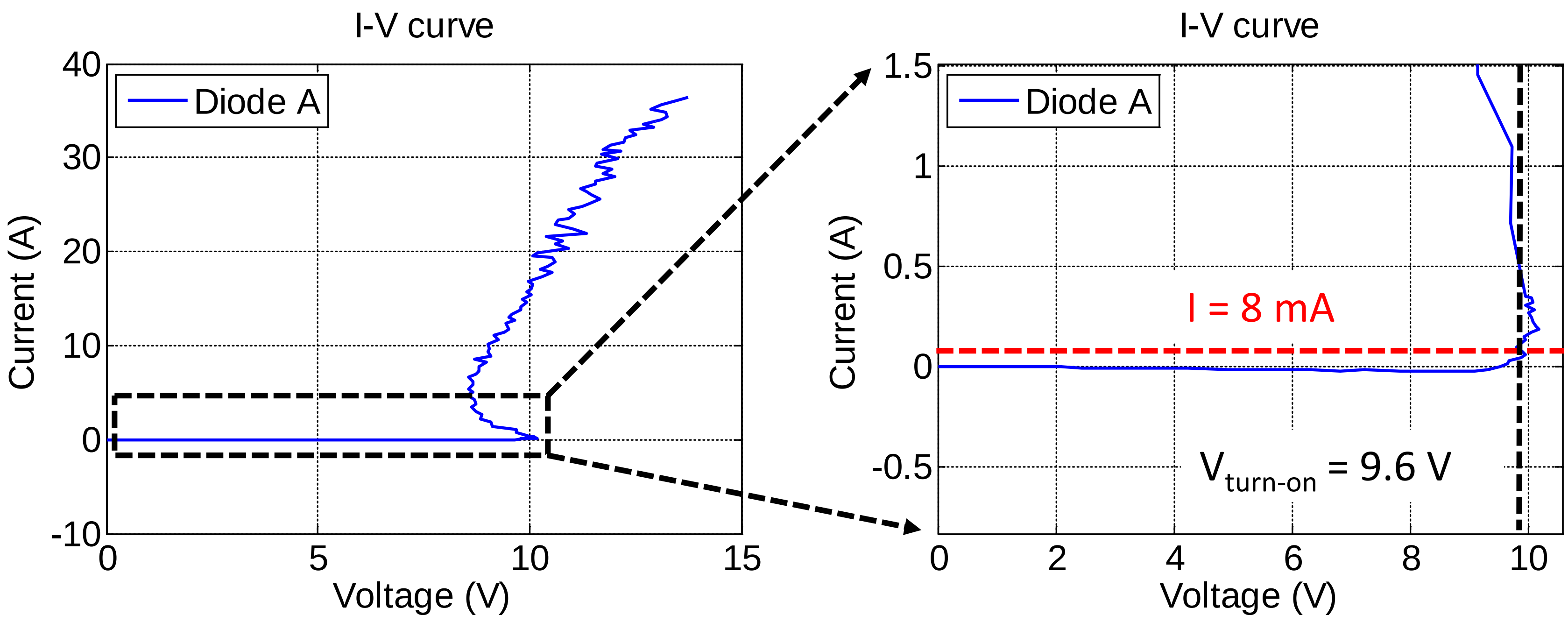
Voltage Undershoot



VF-TLP: Turn-on Voltage

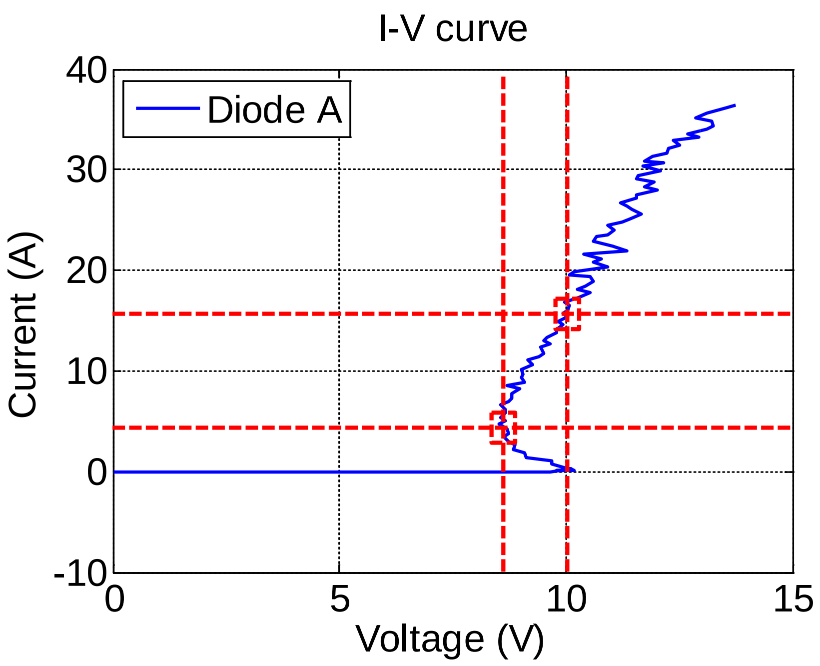
The turn on voltage of the diode is selected from the VF-TLP *IV* curve.

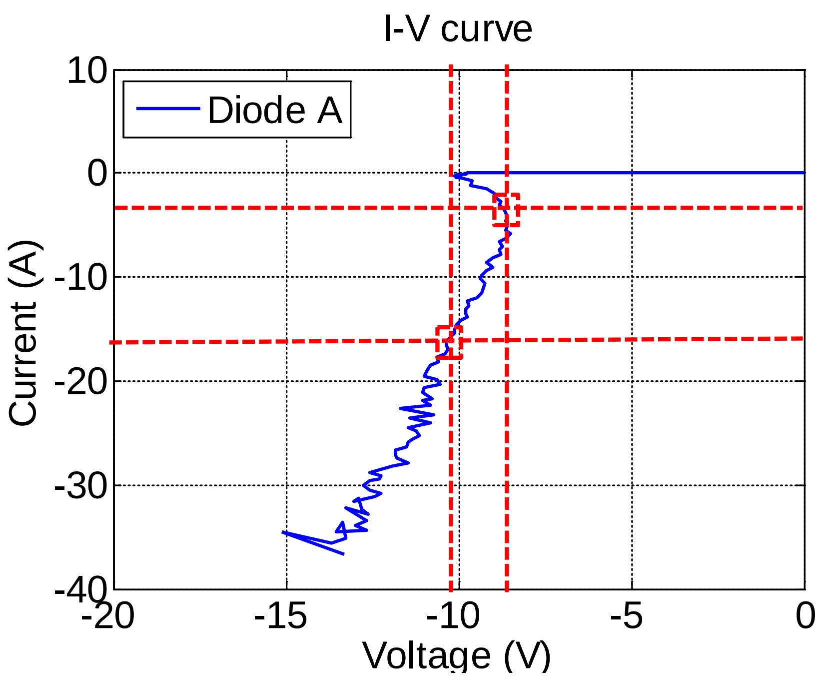
The voltage value at which the diode current is in the range [1-10] mA (obtained from the I-V curve) is selected to be the diode turn on voltage.



VF-TLP: Dynamic Resistance

The dynamic resistance is calculated from the device *IV* curve. The line drawn between the two points at 4 A and 16 A are used.



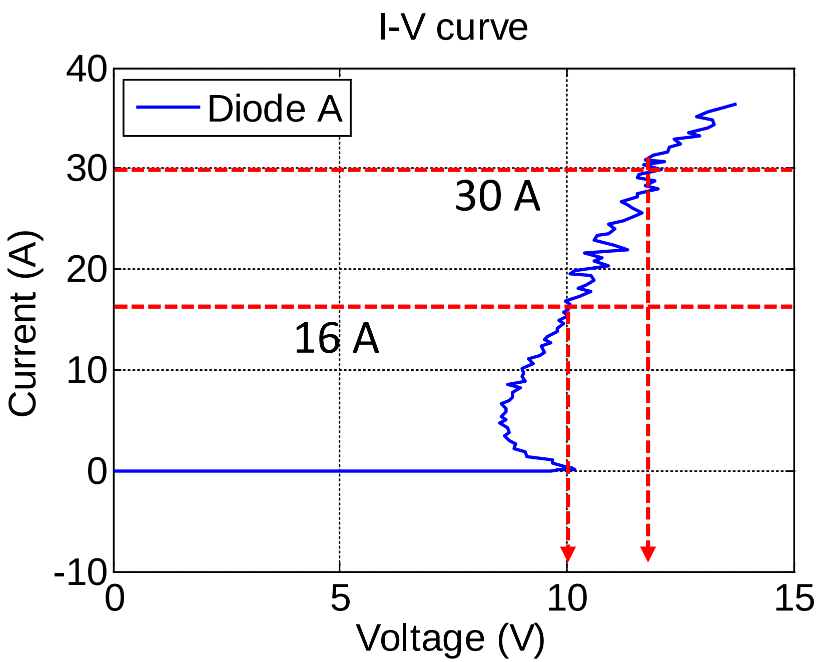


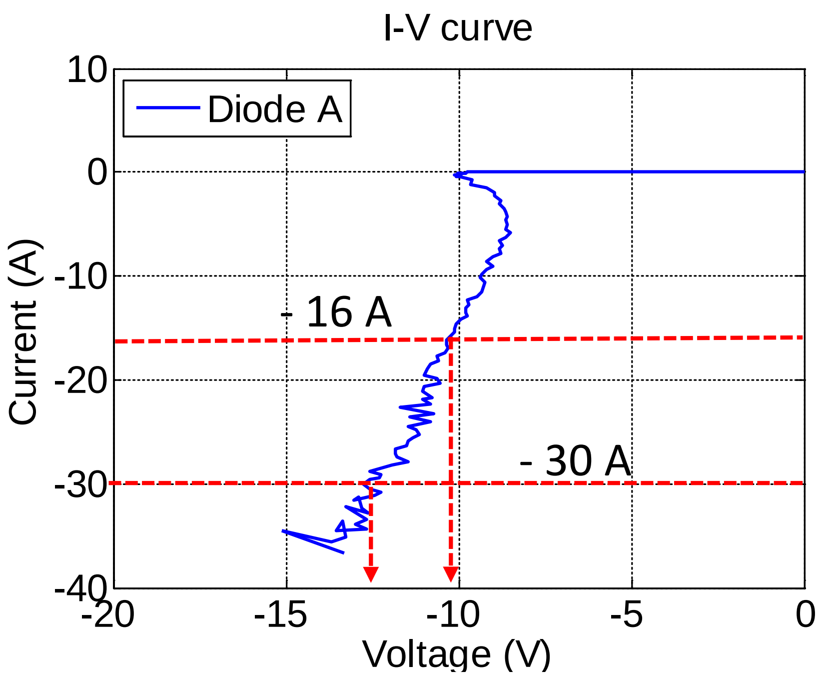
$$R_{dyn} = \frac{V_{16} - V_4}{I_{16} - I_4}$$

VF-TLP: Clamping Voltage

The clamping voltages for I_{tlp} = 16 A and I_{tlp} = 30 A are obtained from the diode *IV* curve

➢ This clamp value is reported for both polarities (positive and negative)

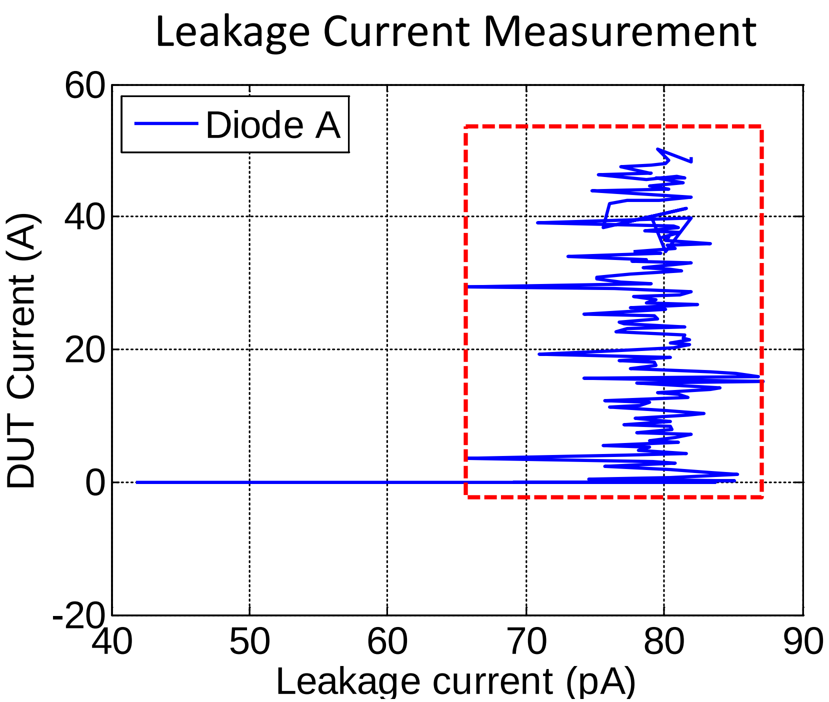




VF-TLP: Device Failure Threshold

This parameter is determined by the device leakage current. The failure criterion is chosen to be a 10x increase in the DC leakage.

If the test does not show a device failure then the maximum diode current is reported.



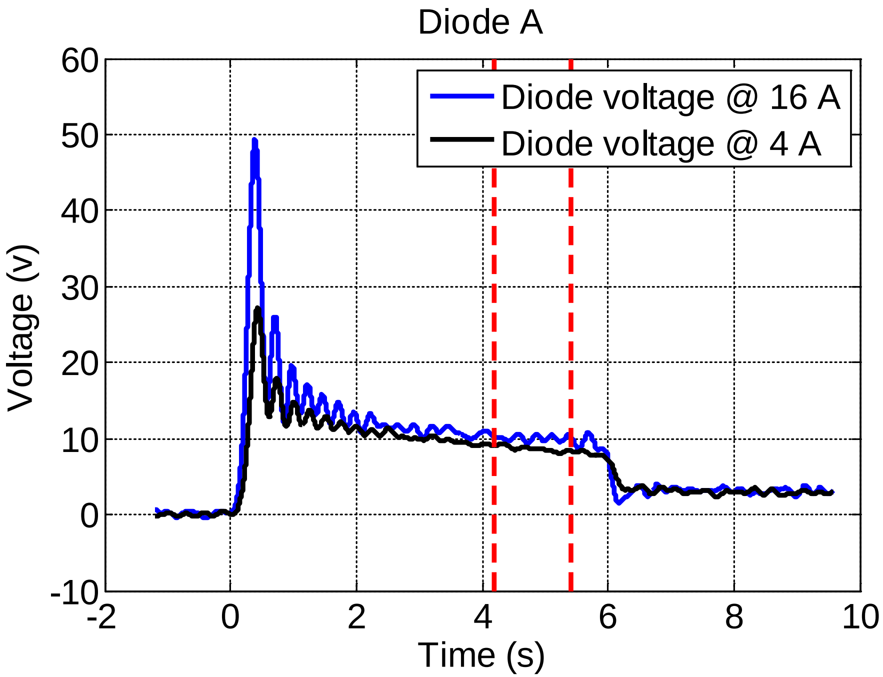
The device leakage current is measured by applying a constant voltage using a source-measure unit after each TLP pulse is applied. The leakage current is plotted here against the test current.

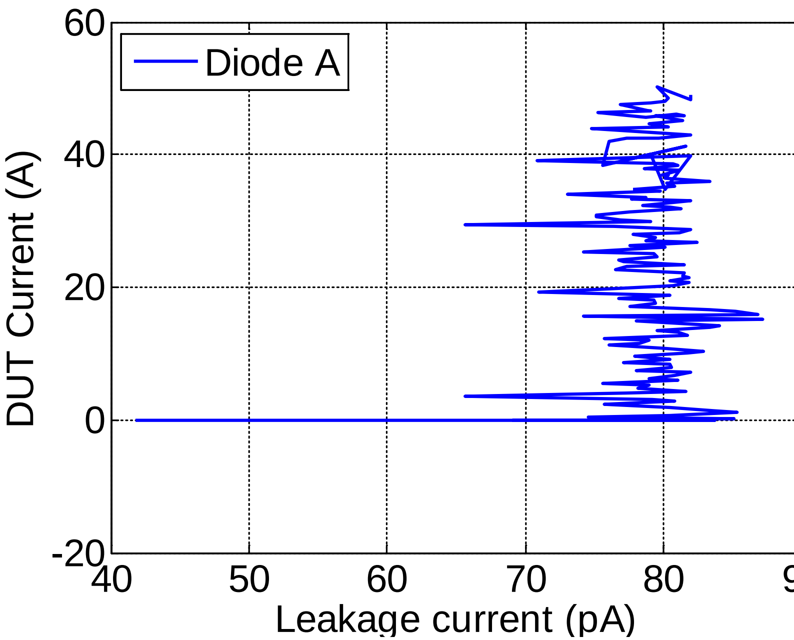
VF-TLP Test Example (Diode A): Part 1

The VF-TLP data is processed in Matlab and the following parameters values are calculated from the diode current and voltage curves. The red dotted lines, represent the 70-90% measurement window of the 6 ns pulse.

- Turn on Time @ 4 A: **1.6 ns**
- Turn on Time @ 16 A: **0.83 ns**

At the maximum TLP source voltage of 2.5 kV, the diode current reaches 50 A, but the leakage current remains in the range of pA, indicating that the device did not fail.

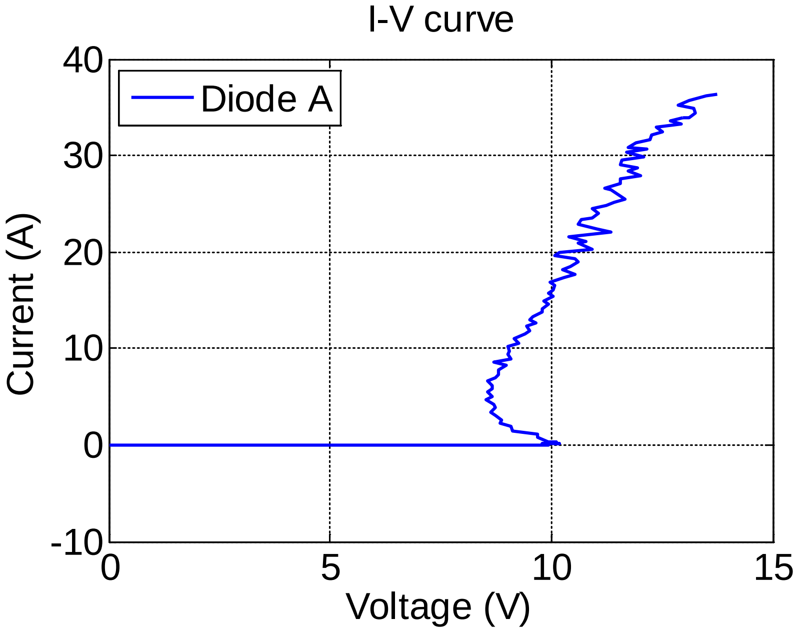




VF-TLP Test Example (Diode A): Part 2

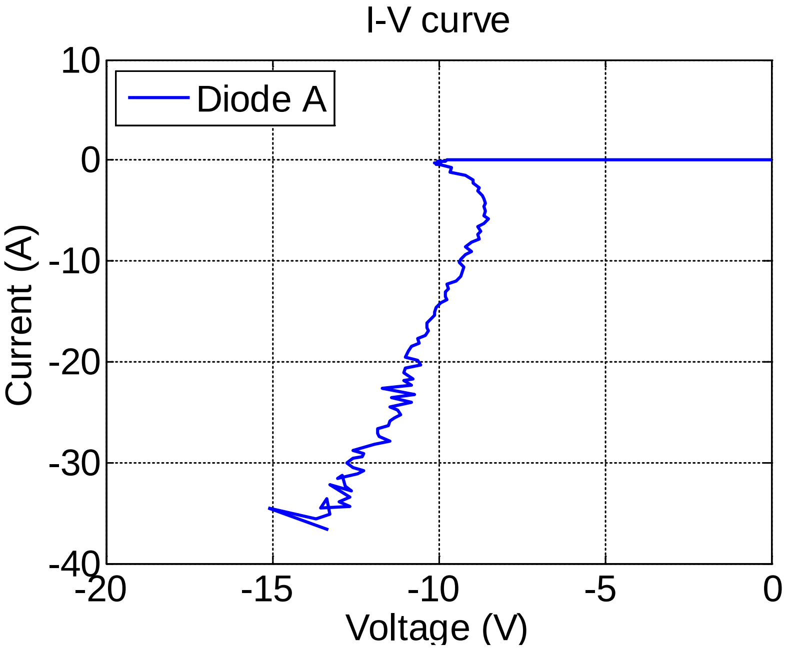
Positive

Turn on voltage: **9.6 V**
Dynamic resistance : **0.11 Ω**
Clamp voltage @ 16 A: **10 V**
Clamp voltage @ 30 A: **12.1 V**



Negative

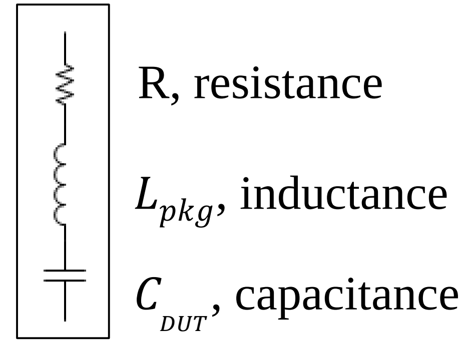
Turn on voltage: **-9.6 V**
Dynamic resistance: **0.13 Ω**
Clamp Voltage @ -16 A: **- 10.3 V**
Clamp Voltage @ -30 A : **- 12.8 V**



VNA Test Setup & Steps

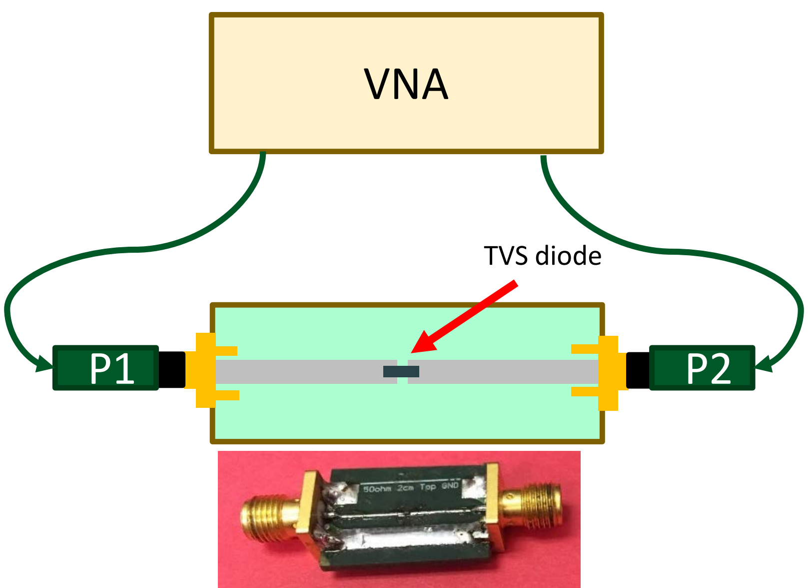
Device s-parameters are measured by VNA to obtain the total diode capacitance, package inductance, and insertion loss at 2.5 GHz, 5 GHz and 10 GHz when placed in shunt to a trace.

- Capacitance is first measured via a S21 → Z21 measurement using test fixture #1.
- S21 is again measured for test fixture, directly yielding the insertion loss.
- An S21→ Z21 conversion is then performed and the previously measured capacitance value is used to calculate the package inductance from any visible resonances.

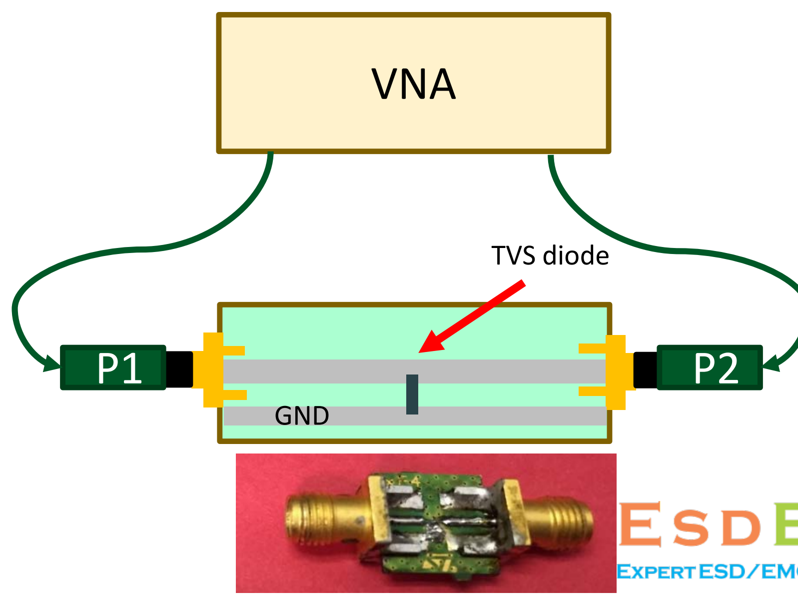


Diode equivalent circuit in passive state

Test Fixture #1



Test Fixture #2



VNA: Capacitance Measurement

To extract the TVS diode capacitance, Z_{21} is calculated from the measured S-parameter set. The VNA is calibrated to end of coaxial cables. From $|Z_{21}|$, we choose region that is dominated by capacitance and perform the following calculation:

$$Z_{ab}^{tr} = \frac{2\sqrt{Z_{0a}Z_{0b}}}{S_{ab}} - (Z_{0a} + Z_{0b})$$

$$C_{DUT} = \frac{1}{2\pi f\left|Z_{ab}^{tr}\right|}$$

One 0402 capacitor of value **1.8pF** was measured the S-parameters and apply the described method to verify.

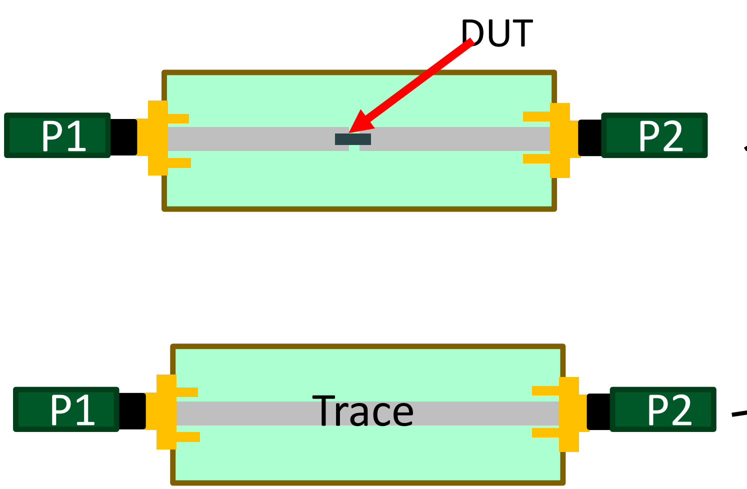
A data point at 50 MHz was used. This calculation returns capacitance of 1.8024pF, which is in good agreement with the stated value.

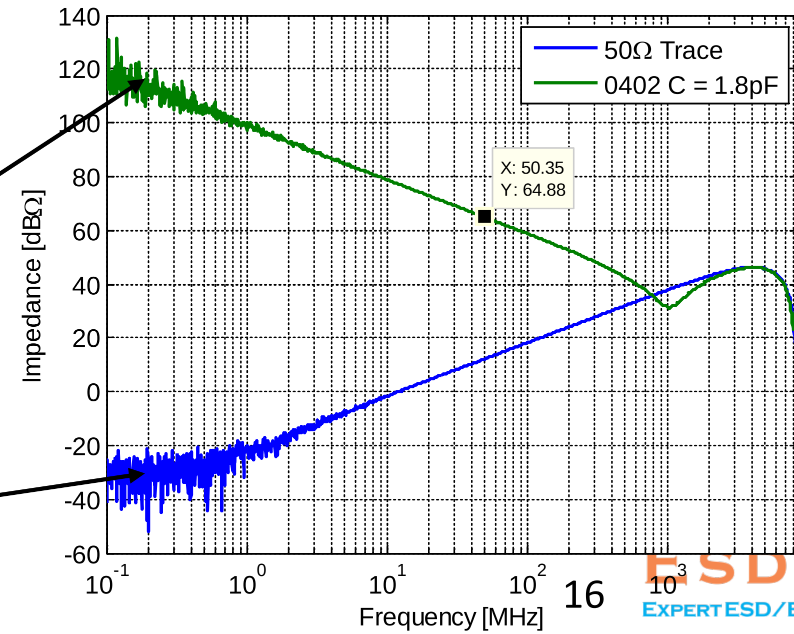
Z_{ab}^{tr} - Equivalent Impedance in **transmission** measurement

S_{ab} - S_{21} between port **a** and port **b**

Z_{0a} - Characteristic impedance of port **a**

Z_{0b} - Characteristic impedance of port **b**





VNA: Diode A – Capacitance

The diode is soldered in series orientation on the microstrip test fixture. The capacitance is calculated at a frequency of 50 MHz from the value Z_{ab}^{tr} at 50 MHz.

$$C_{DUT} = \frac{1}{2\pi f \left| Z_{ab}^{tr} \right|}$$

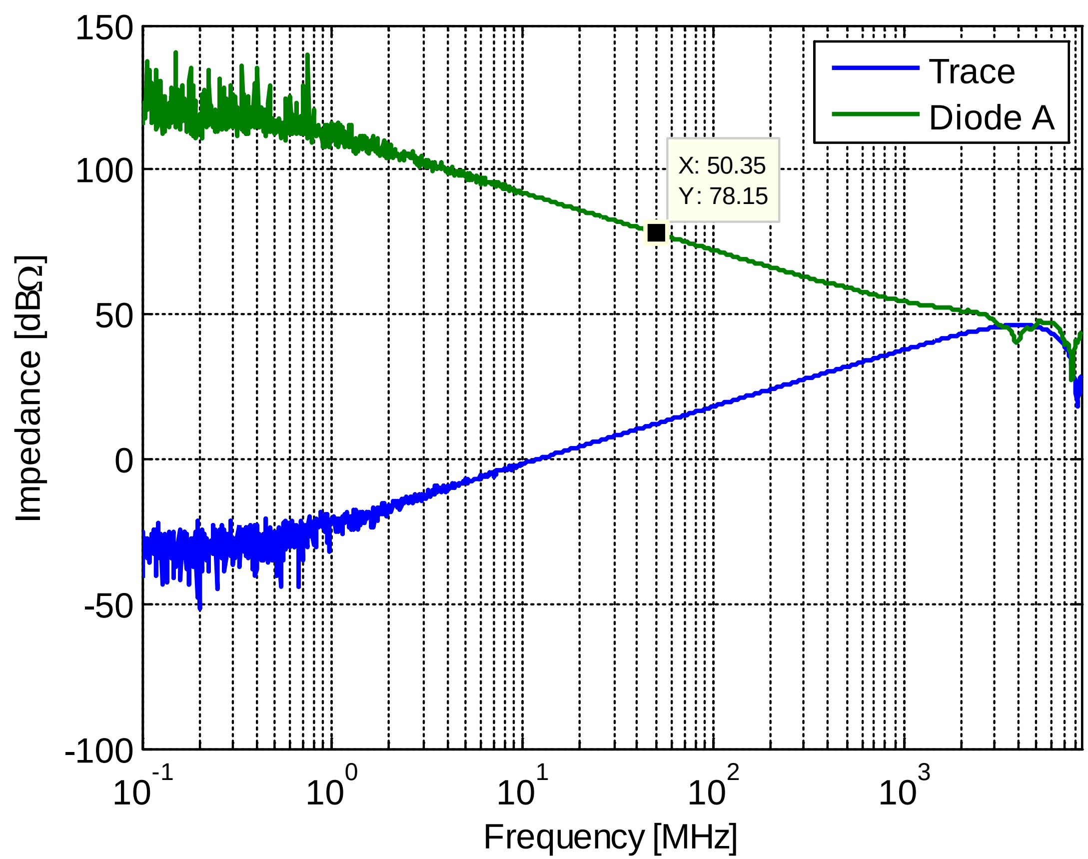
Z_{ab}^{tr} - Equivalent Impedance in **transmission** measurement

S_{ab} - S21 between port **a** and port **b**

Z_{0a} - Characteristic impedance of port **a**

Z_{0b} - Characteristic impedance of port **b**

Capacitance = 3.96 pF



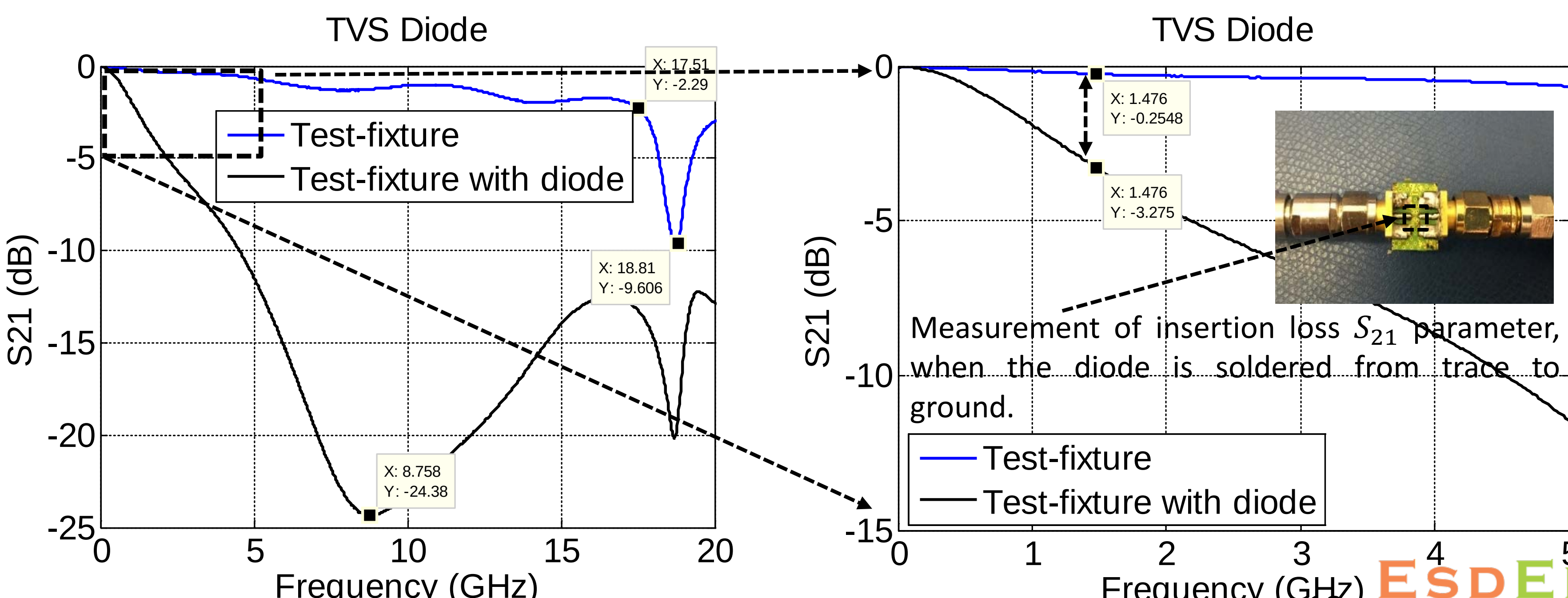
VNA: Insertion Loss & Package Inductance

The blue curve represents the insertion loss of the standalone test fixture #2 and is observed to have a useful operational range between 0 and 17.5 GHz, beyond which a strong resonance is observed.

The black curve represents the same measurement but with the TVS device soldered from the trace to a nearby ground structure. This introduces a resonance at ~8.8 GHz. Using the previously measured capacitance value (3.96 pF), the inductance is calculated by:

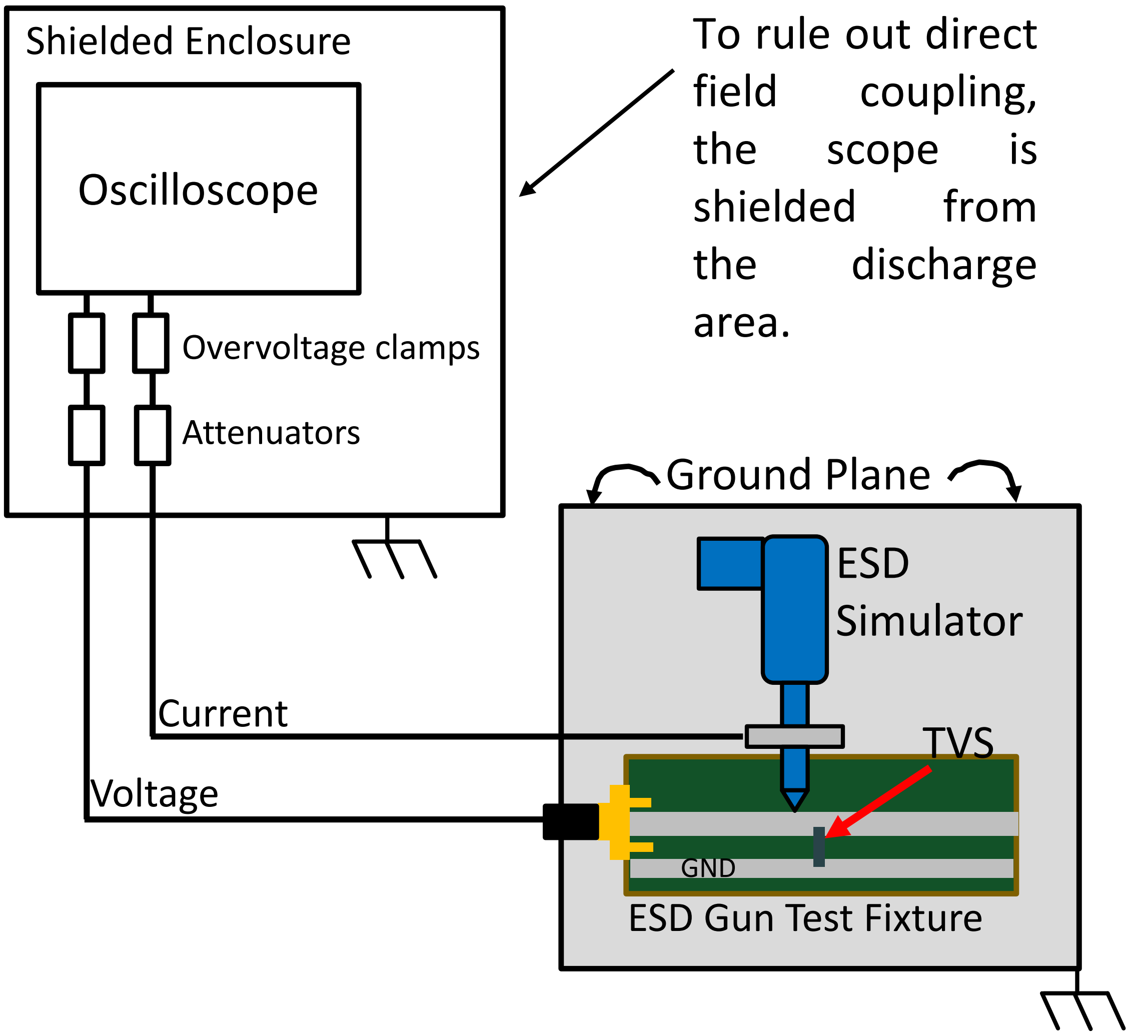
$$f_{resonance} = \frac{1}{2\pi\sqrt{L_{pkg} * C_{DUT}}} \rightarrow L_{pkg} = 0.08\text{ nH}$$

The useful bandwidth of the diode is defined as the 3 dB insertion loss frequency which is seen to be ~1.4 GHz.



ESD Simulator Discharge Test setup

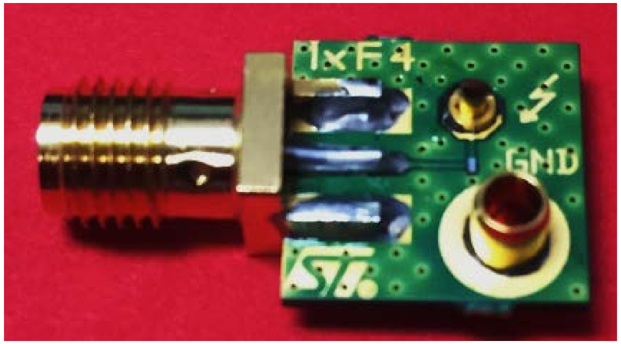
The ESD simulator discharge test is performed to obtain peak voltage at the TVS diode for **8 KV Contact discharges** during both positive and negative discharges.

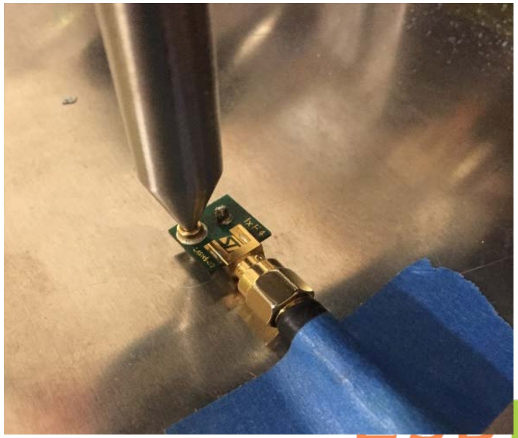


To rule out direct field coupling, the scope is shielded from the discharge area.

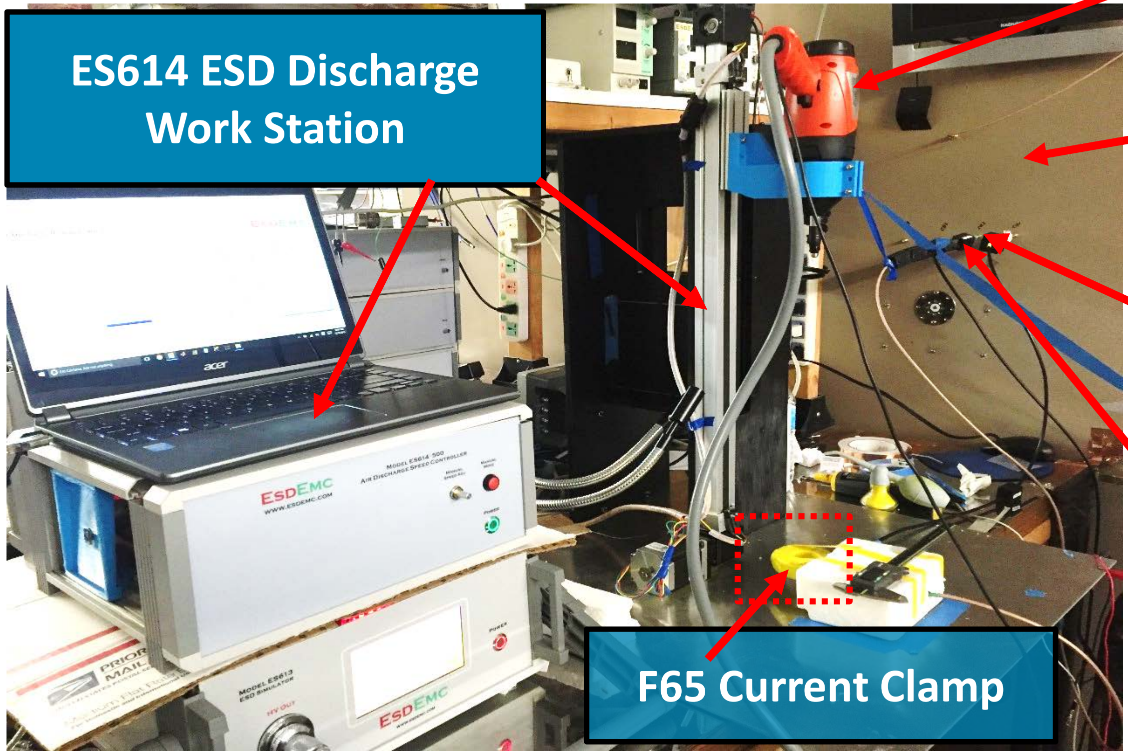
ESD gun is discharged into the signal trace of the test fixture.

ESD Gun Test Fixture





ESD Simulator Discharge Test System



Product link:

(1) ES613 ESD Simulator:
https://www.esdemc.com/products/esd-simulators/es613-esd-simulator/

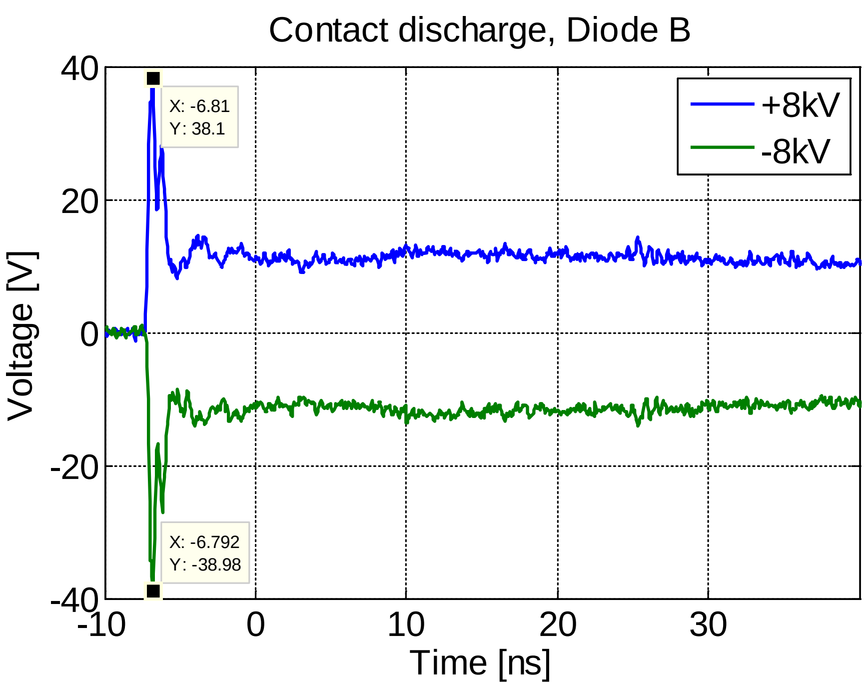
(1) ES614 ESD Air Discharge work Station:
https://www.esdemc.com/products/system-level-esd-test/es614-series-esd-air-discharge-work-station/

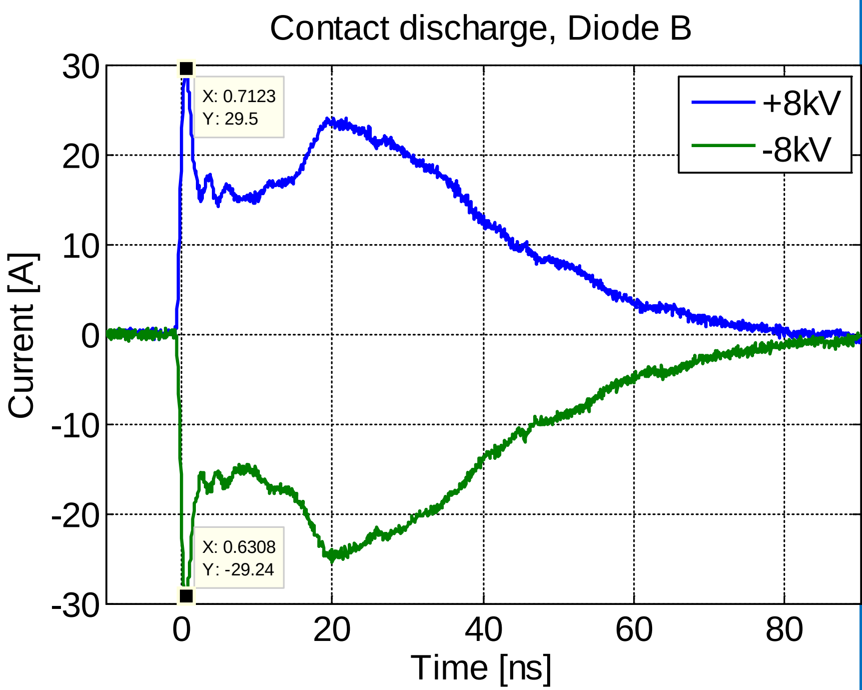
ESD Simulator Discharge Waveforms

Output voltage is measured using a coaxial cable probe.

Discharge current is measured by an F-65 current clamp.

$V_{peak,pos}$	38.10 V
$V_{peak,neg}$	-38.98 V
$I_{peak,pos}$	29.50 A
$I_{peak,neg}$	-29.24 A

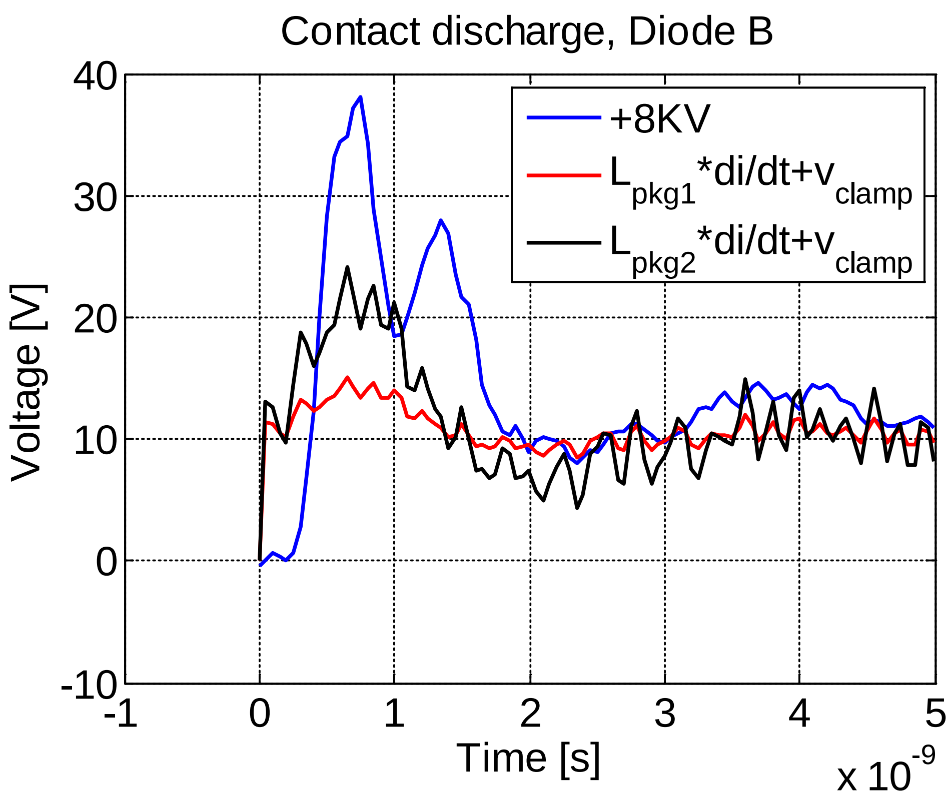


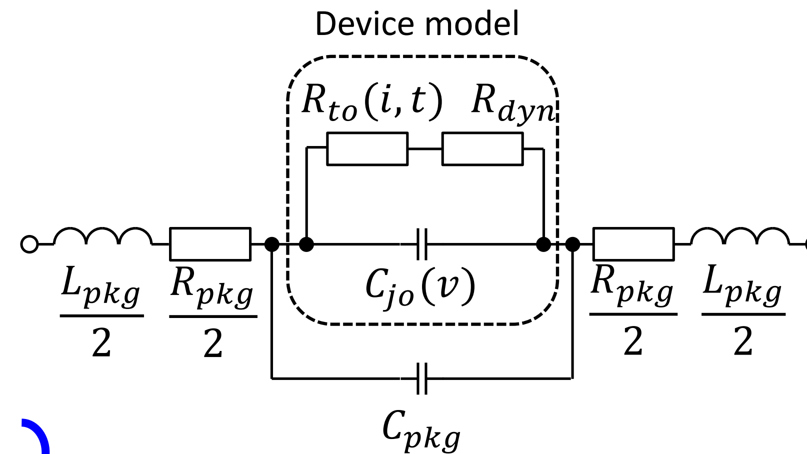


ESD Simulator Discharge Peak Voltage

The transient voltage contribution from the package inductance is calculated from the measured device current.

The DC voltage V_{clamp} is added to make a similar comparison to the measured voltage waveform.





We term the measured voltage overshoot the "effective inductance"

This range of calculated overshoots is due only to the package

Clearly, the package inductance alone cannot account for all of the observed effective inductance and some additional factors influence this first overshoot.

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Results Comparison

Part Number	Peak Clamp @8KV (Reverse) (V)	Peak Clamp @8KV (Froward) (V)	TLP Clamp @16A (Reverse) (V)	TLP Clamp @30A (Reverse) (V)	TLP Clamp @16A (Forward) (V)	TLP Clamp @30A (Forward) (V)	R-Dyn (Forward) (Ω)	R - Dyn (Reverse) (Ω)	Turn on voltage (V)	Turn On time @ 4A (ns)	Turn On time @ 16 A (ns)	C-j max (pF)	Frequency Bandwidth (GHz)	Insertion loss @ 2.5 GHz (dB)	Insertion loss @ 5 GHz (dB)	Insertion loss @ 10 GHz (dB)	L-pkg max (nH)
B_Diode A	-57.4	56.2	-10.3	-12.8	10	12.1	0.11	0.13	9.6	1.6	0.83	0.39	13.6	0.3	0.3	0.8	N.A.
B_Diode B	-39.0	38.1	-11.6	-13.3	11.6	13.4	0.12	0.13	8.4	0.34	0.44	3.96	1.5	5.3	11.8	24.7	0.1
B_Diode C	-140.7	140.8	-18.5	-23.2	17.1	22.1	0.41	0.54	9.2	0.99	0.86	0.24	> 17	0.2	0.2	0.6	N.A.
B_Diode D	-135.3	136.5	-6.9	-9.8	7.5	11.4	0.31	0.22	17.2	1.69	1.21	0.21	>17	0.2	0.2	0.4	N.A.
B_Diode E	-124.0	122.6	-16.5	-22.9	16.3	22.4	0.56	0.56	8.9	1.09	0.48	0.23	13.5	0.3	0.3	0.8	N.A.
B_Diode F	-194.3	195.9	-21.1	-34.2	22	33.6	0.79	0.69	10.5	1.57	1.21	0.22	>17	0.3	0.3	0.7	N.A.
B_Diode G	-157.7	154.4	-28.1	-43.9	28.8	44.4	1.10	1.06	9.1	1.04	1.29	0.47	>17	0.2	0.2	0.5	N.A.
U_Diode H	-198.4	**165.4**	**-12.1**	**-19.7**	15.5	22.3	0.47	**0.62**	7.5	1.24	1.32	0.57	10.1	0.6	0.9	2.9	N.A.
U_Diode I	**-116.2**	106.1	**-9.5**	**-15.1**	13.3	17.8	0.32	**0.46**	8.03	0.47	0.61	0.22	>17	0.2	0.2	0.6	N.A.
U_Diode J	**-140.3**	85.7	**-6.5**	**-9.7**	20.7	22.4	0.12	**0.29**	18.12	0.42	0.42	4.40	4.1	2.4	3.5	13.5	0.045
U_Diode K	**-110.5**	102.3	**-8.4**	**-13.4**	13.1	17.1	0.29	**0.42**	7.98	0.72	0.88	0.81	9.8	0.6	1.1	3.2	N.A.
U_Diode L	-92.8	**57.7**	**-3.7**	**-5**	3.6	4.9	0.13	**0.15**	18	1.54	0.64	0.49	11.8	0.4	0.4	1.2	N.A.
U_Diode M	**-19.3**	34.2	**-7.8**	**-13.9**	15.9	23.5	0.55	**0.43**	7.02	0.5	0.55	35.88	0.18	25.8	26.7	20.8	0.054
U_Diode N	**-75.3**	82.0	**-6.1**	**-10**	8.6	11.5	0.17	**0.29**	8.08	1.04	1.5	0.41	9.9	0.4	0.6	3.1	N.A.
U_Diode O	**-102.8**	143.3	**-7.7**	**-13.1**	13.9	20.6	0.40	**0.37**	9.55	1.77	1.04	0.39	10.6	0.5	0.5	2.4	N.A.
U_Diode P	**-38.6**	42.1	**-5**	**-8**	11.3	14.5	0.29	**0.24**	5.39	0.44	0.61	39.96	0.18	18.5	9.3	6.5	0.25
U_Diode Q	**-98.6**	106.1	**-11.6**	**-19.3**	16.6	23.1	0.47	**0.57**	8.23	0.83	0.97	0.80	9.6	0.6	0.7	3.6	0.13

* Part number: 'B_' stands for Bidirectional diodes, 'U_' stands for Unidirectional diodes

** Bolded numbers describe the non-TVS behaviors of unidirectional devices

*** Many L_{pkg} values are listed as NA because no resonances are observed below 17 GHz

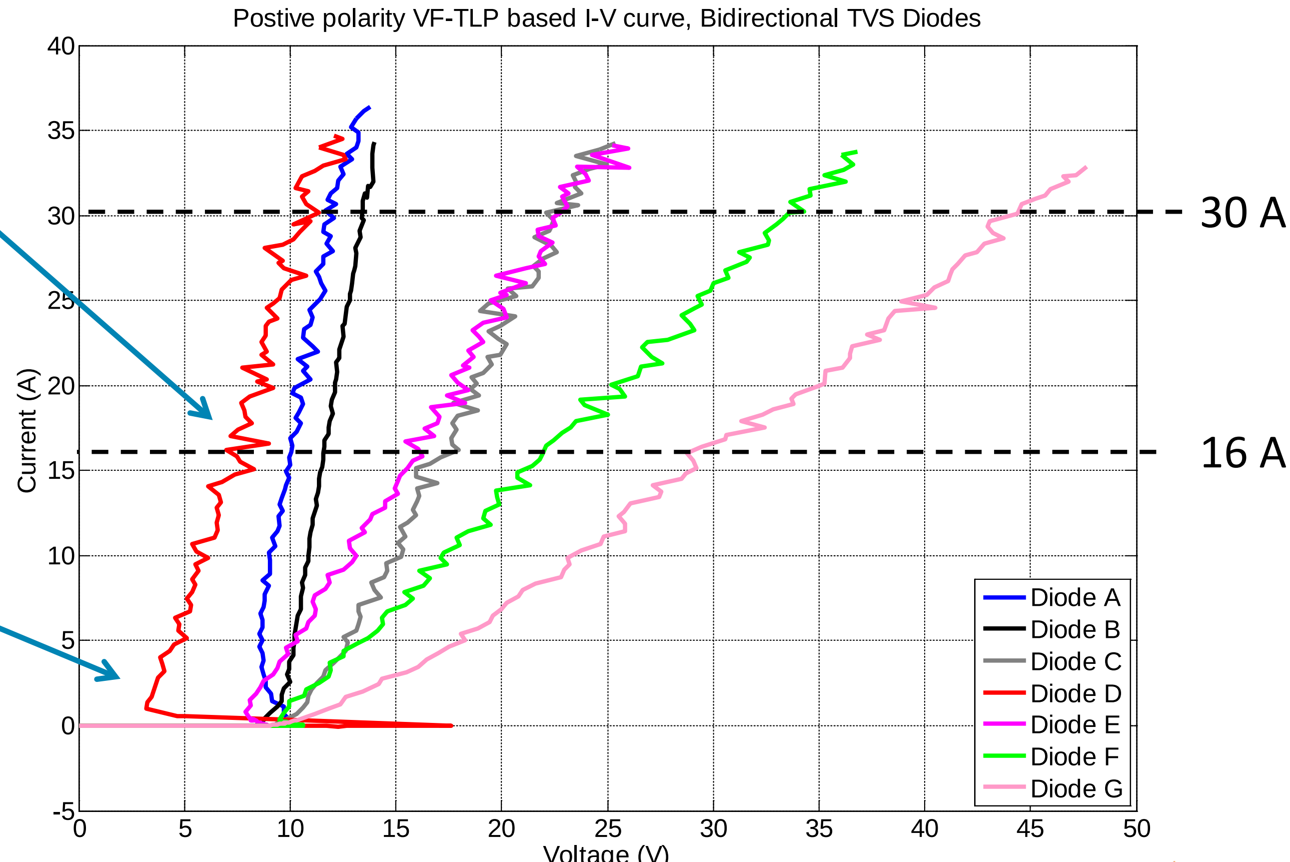
**** No device failures were recorded

Application: VF-TLP *IV* curve data

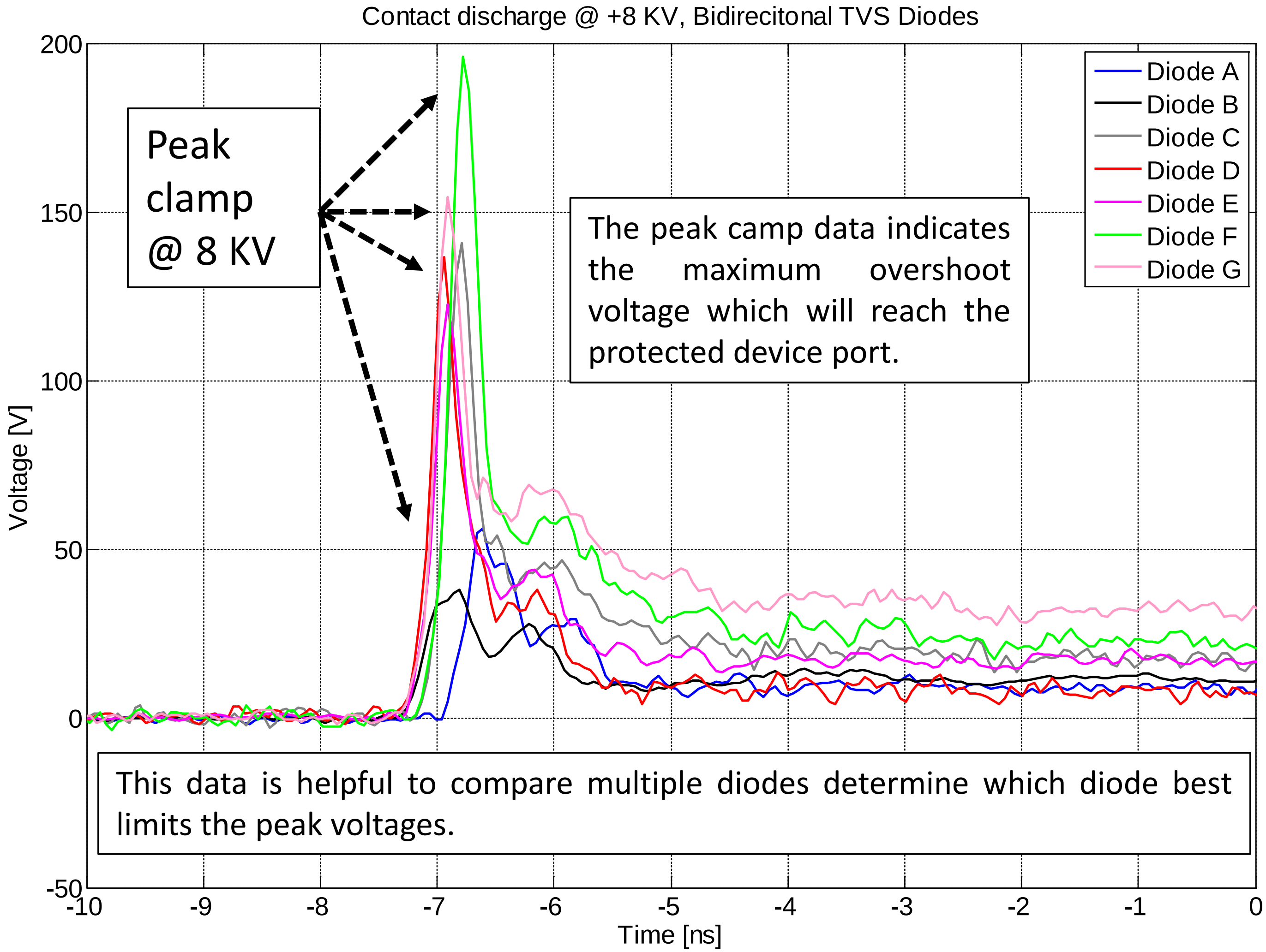
The *IV* curve of bidirectional devices for positive polarity when plotted together, gives a quantitative comparison of various TVS devices, when selecting a device for an end application. The protected device max damaging current limit or the max voltage limit can be one of the diode selection criteria. SEED simulation is probably needed to understand the effectiveness of the selected diode for a specific circuit application.

Snapback devices exhibit lower TLP clamp voltages at both 16 A and 30 A when compared to non-snapback devices.

Snap back behavior at the turn of a device

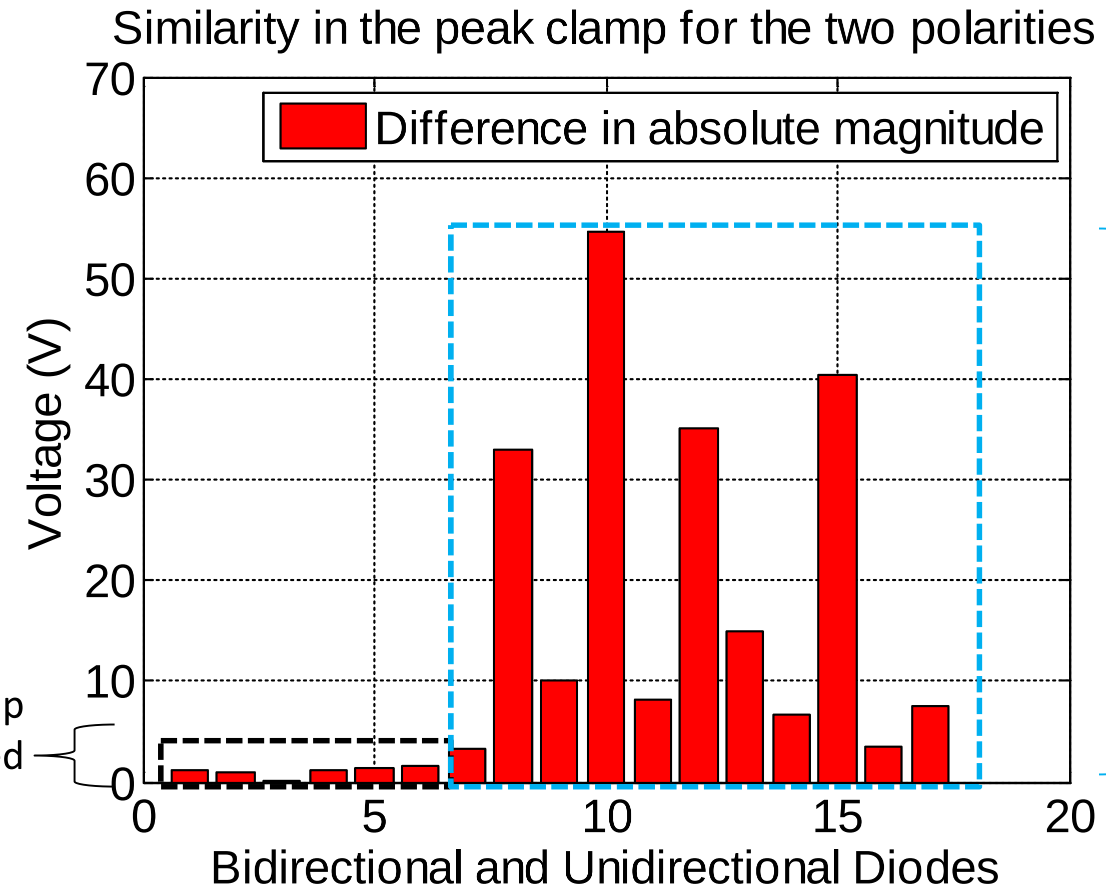


Application: ESD Gun measurement data



Application: ESD Gun measurement data

The difference in peak clamp @ 8 kV voltages for the two polarities are shown below. Bidirectional diodes show symmetry in the peak clamp data for both polarities, whereas large difference is observed for the unidirectional diodes.



A difference in absolute voltage up to 3.5 V is observed for bidirectional diodes.

A difference in absolute voltage of about 4- 55 V is observed for unidirectional diodes.

Comparison data: diode parameter correlation

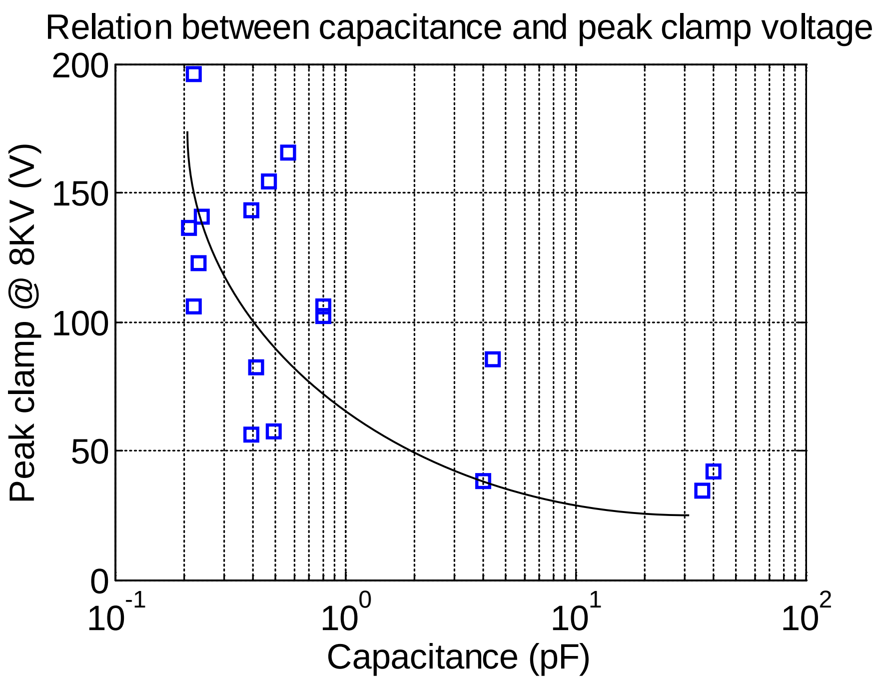
All the data points for a diode parameter are compared with the other diode parameters to understand the trend and relationship between different diode parameters. The curve drawn in the plots, shows the general trend in the correlation of the two data parameters.

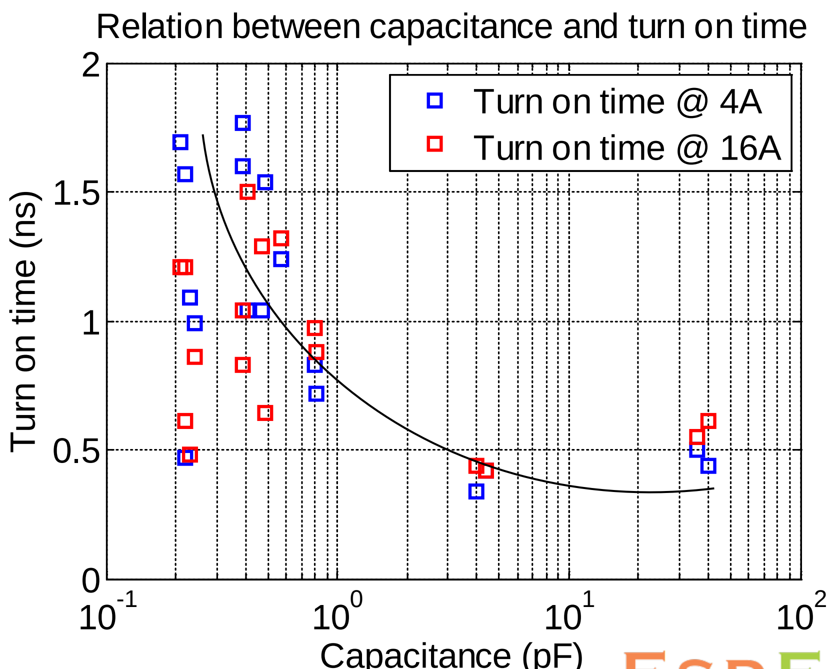
The capacitance and the peak clamp @ ±8 KV data suggests a trend:

- Higher the device capacitance, lower the peak clamp voltage value.

The capacitance and turn on time data suggests that:

- Higher the diode capacitance, faster is the turn on time for the diode. The data suggests a trend, but it needs modelling efforts in simulation software.





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