

Study of CDM, Relay Pogo-Contact First CDM, and CC-TLP Pulses

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Abstract – The recently proposed RP-CCDM testing method is tested alongside the more established CDM and CC-TLP methods on two test ICs to assess the RP-CCDM's efficacy as an alternate test method. High bandwidth analysis of field induced CDM spark events is presented to evaluate higher frequency components of the current.

I. Introduction

A CDM event occurs when the pin of a charged device approaches an external metal object such that the potential difference exceeds the breakdown voltage of the air gap between them. CDM is one of the most common ESD threats in modern manufacturing and usage environments. The current industry standard testing method is the Field Induced CDM (CDM) method governed by the ANSI/ESDA/JEDEC JS-002 standard [1]. Current CDM testers are plagued with repeatability issues due to the variable spark resistance of the air discharge making the practice difficult to standardize [1, 2]. Additionally, decreasing CDM testing voltages increase the pulse-to-pulse variability of the air discharge, causing concern over the ability to meaningfully classify devices at lower voltages [3]. This is becoming increasingly problematic as the necessity for classification at lower levels is becoming greater with advances in IC technology

[2]. Several contact-first CDM methods where a CDM current is induced into the pin through a more controllable method, such as the CC-TLP, LICCDM, and RP-CCDM, have been introduced in an attempt to solve the issue of pulse variability [4, 5, 6].

This work presents a correlation study between the CDM, RP-CCDM and CC-TLP testers on two devices with well-known CDM failure levels and failure mechanisms. The devices are subjected to a series of RP-CCDM and CC-TLP tests with multiple risetimes. The study aims to evaluate the efficacy of the RP-CCDM method and gain insight into the correlation of RP-CCDM and CC-TLP to better understand their potential as replacements for CDM susceptibility testing.

II. CDM and CC-TLP Tester Configurations

A. RP-CCDM Tester

The RP-CCDM, or Relay Pogo-Contact First CDM, is a design of the CDM discharge head that allows the use of a repeatable relay discharge while largely preserving the design parameters of the JS-002 standard. Figure 1 shows a cross section of the RP-CCDM head.

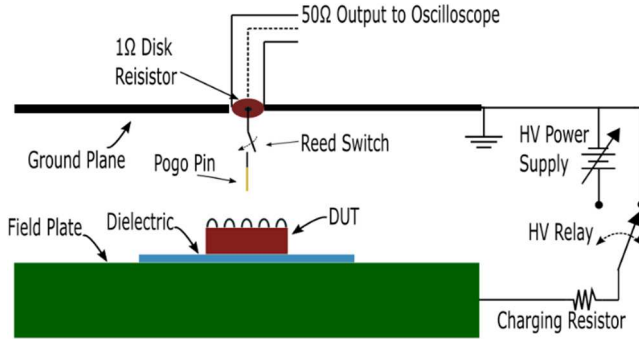


Figure 1: RP-CCDM Discharge Circuit

As shown in Figure 1, the RP-CCDM uses the field charging method and a similar discharge path to the one specified in the JS-002 standard. To charge the device, the pogo pin of the RP-CCDM ground plane is lowered to contact the DUT pin, then the field plate is brought to the specified charge voltage. To discharge, the reed switch is closed and the current primarily flows up the pogo pin, through a high bandwidth $1\ \Omega$ resistor, and returns via the ground to field plate and DUT capacitances. A more detailed testing procedure for the RP-CCDM is presented in [6].

The RP-CCDM prototype head used for stressing devices in this study was found to adhere to the discharge waveform parameters specified in the JS-002 standard. The RP-CCDM prototype was also found to have a strong correlation in peak currents to the peak values measured with a CDM head across a range of coins with varying C_{DUT} values.

B. ACRP-CCDM Test Setup

The RP-CCDM and CDM test are different in two key aspects that could be the source of correlation issues. First, the RP-CCDM spark takes place in a controlled environment free of air. This difference results in a much more reproducible spark

environment that reduces the variability of the peak current when compared to air discharge CDM and enables testing below 100 V [6]. The altered spark environment may also influence the risetime and result in less damping of the system due to a smaller series spark resistance value. Second, the geometry of the RP-CCDM head is different from that of the CDM to accommodate the reed switch. Specifically, the pogo structure is no longer uniform in thickness and longer than in CDM, which will affect the inductance of the discharge path. To further investigate the role of these two variables the “Always Closed” RP-CCDM (ACRP-CCDM) test method was implemented. This test method uses the existing RP-CCDM test setup but alters the testing procedure to close the reed switch in the pogo pin prior to descent such that a CDM-like air spark is created. This method removes the reed switch spark variable and reveals differences between CDM and RP-CCDM based on the test head geometry alone.

To evaluate differences in the rising edge, or any other part of the current waveform, RP-CCDM, ACRP-CCDM, and CDM tests were performed using a 23 GHz bandwidth Tektronix MSO72304DX oscilloscope and a low loss measurement chain. The insertion loss of the measurement chain, shown in Figure 2, was less than 2 dB up to the 23 GHz measurement bandwidth of the oscilloscope. The same model of disk resistor was used for the construction of both heads with the resistive sheet facing away from the pogo-pin, this type of disk resistor has been characterized up to 26.5 GHz in [7]. The DC resistance value was used for current measurement scaling.

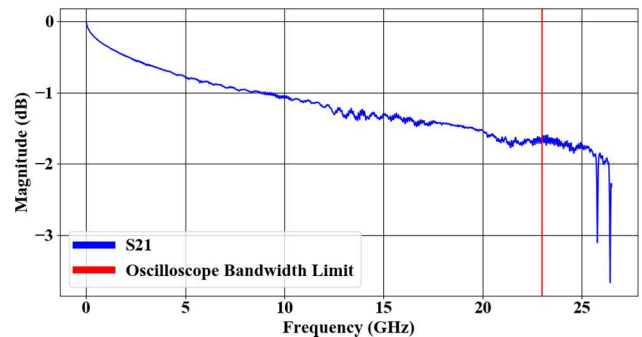


Figure 2: Insertion loss of measurement chain used for CDM and RP-CCDM

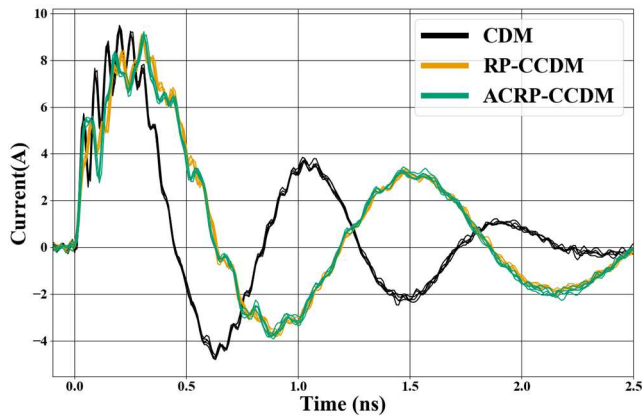


Figure 3: High bandwidth RP-CCDM and CDM current measurements.

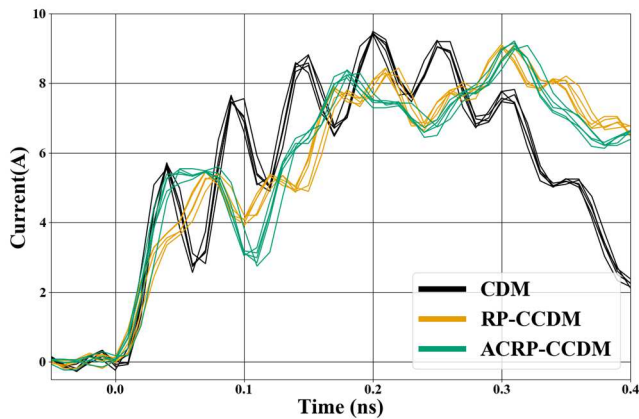


Figure 4: Magnified view of rising edge captured in high bandwidth comparison measurement.

Figure 3 displays the five highest peak current pulses captured from a set of fifty discharges on a small JS-002 verification module at TC500. These pulses represent the lowest spark impedance discharges for each tester. The initial rising edge of the CDM and RP-CCDM pulses is observed to be similar, although the CDM rising edge reaches a higher peak in the first 50 ps and the RP-CCDM reaches a higher peak in the first 80 ps. The ACRP-CCDM current measurement has a rising edge more similar to that of the CDM pulse, possibly indicating a relationship between the rising edge and the air spark event, whereas for the rest of the measurement duration the ACRP-CCDM pulse matches the curve of the RP-CCDM current indicating a relationship with the test head geometry. The risetime of the RP-CCDM does not exhibit any characteristics that indicate a faster risetime than its air spark counterparts. The RP-CCDM slew rate may be faster on average, however, due to degradation in the CDM slew rate

during discharges with high series spark resistance. Figure 5 displays the frequency spectrum of each pulse shown in Figure 3.

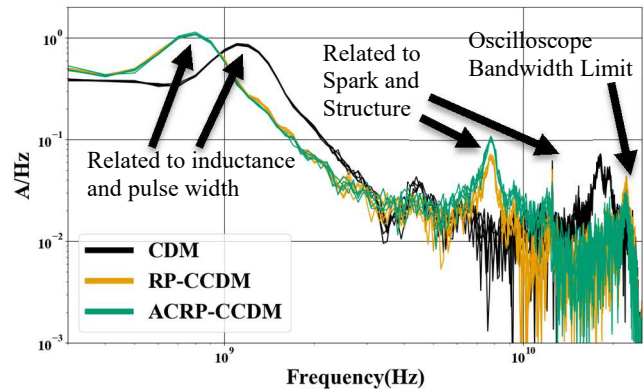


Figure 5: Spectrum of High Bandwidth RP-CCDM and CDM Measurements, displayed on log-log scale.

In [7], it was observed that the high frequency content seen in the CDM and RP-CCDM spectrum is likely related to the pogo pin length and the disk resistor. As shown in Figure 5, the high frequency content observed in the RP-CCDM spectrum is quite similar to the content seen in the ACRP-CCDM spectrum, indicating that the RP-CCDM relay spark does not introduce any unwanted resonances. Whether the current measurements in Figure 3 and the structure resonances seen in Figure 5 are indicating the true current magnitude that is traveling through the IC pin during a CDM stress is not yet fully understood but is currently being investigated. The presence of the high frequency current components that occur in field induced CDM events could be an important factor in determining the efficacy of alternate test methods on sensitive ICs.

C. CC-TLP Test Setup

The CC-TLP method utilizes a VF-TLP pulse into to a single IC pin and a capacitively coupled return path to create a CDM equivalent stress [4]. CC-TLP is a contact-mode tester and as such has the advantage of having much lower pulse to pulse variability than a standard CDM test with an air spark. The CC-TLP method also allows correlation between peak current levels and pulse width settings to CDM stress parameters which can be used to evaluate CDM type failure modes [8, 9]. In this study, two CC-TLP setups were used for testing. The first tester used to perform testing

at IFX, uses a circular ground disk with a diameter of 5 cm. The length of the probe tip is adjusted to 0.3 mm [10]. A TLP system with 1 ns pulse width and 100 ps risetime is connected as excitation source. The second CC-TLP tester, manufactured by and used to perform testing at ESDEMC, uses a test head with a square, rather than circular, ground plate the same size as a JS-002 CDM tester's ground plate. The length of the probe tip is adjusted to 0.5 mm. The bandwidth of both CC-TLP measurement chains were limited by the pick-tee cutoff at approximately 10 GHz. Both testers integrate S-parameter compensation of the measurement chain in software. The same pulse parameters were used for both testers. A "dummy" device was used to determine the charging voltage necessary to achieve the desired peak current on each pin of each device tested.

III. Correlation Study

A. Device Information

Table 1: Description of test devices used in correlation study.

	Package	Process Technology
Device A	TSSOP-Wirebond	130 nm CMOS
Device B	BGA-eWLB	130 nm CMOS

Two different test devices are used for the correlation study of RP-CCDM, ACRP-CCDM, CC-TLP and CDM in terms of the failure level. Both devices are designed in 130 nm CMOS technology. Device A is packaged in a TSSOP, device B as eWLB. The expected failure mode is the excess of a critical potential level leading to gate oxide damage at one or more transistors. The failure mechanism of device A is a GOX failure triggered by a cross-domain issue and is located at an internal interface in the core. Device B shows several GOX failures and increased IDDQ currents after the damage occurring at the transistors on the edge of the digital core.

B. Transmission Line Connected Pins

As observed in measurements on the JS-002 verification modules, the peak current of the RP-CCDM and CDM testers was measured to be

nearly identical on a reference connected pin of the device as seen in Figure 6. However, this relation was found to not hold across all pins on device B.

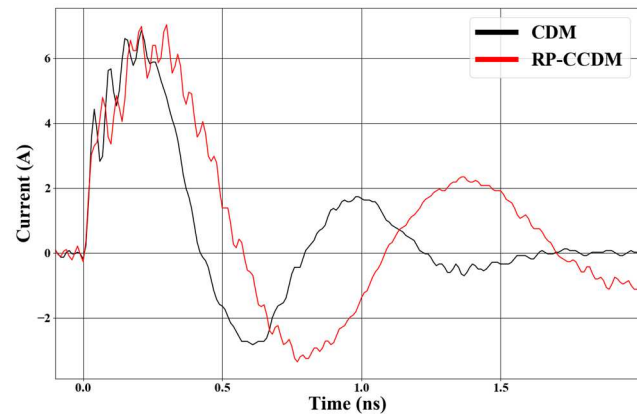


Figure 6: Comparison of CDM and RP-CCDM on a reference connected pin of device A during qualification test.

The most sensitive pins on device B are high-speed I/O pins connected to the die via impedance controlled, transmission line (TL), traces, such as shown in Figure 7.

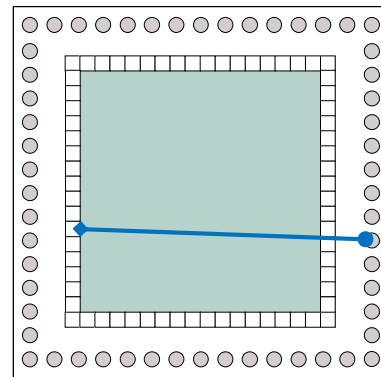


Figure 7: Schematic sketch of Device B. A long TL (blue) connects the ball with the pad leading across the silicon.

In Figure 8 two curves of a TDR measurement in a CC-TLP setup are shown. The probe tip of the CC-TLP test head is connected to the chip, so that the current path to the die can be analyzed such as shown in [11]. Once the current wave reaches the die, the capacitance formed by the package and die to the ground disk of the test head is charged and marks the end of the transmission path. This method enables to measure delay times of single pins. In case of a pin with a corresponding ball in the direct vicinity of the die pad the delay due to the transmission path can be neglected (Fig. 8, green curve). For the second pin the connected

transmission line forms a stable impedance for about 120 ps (Fig. 8, blue curve).

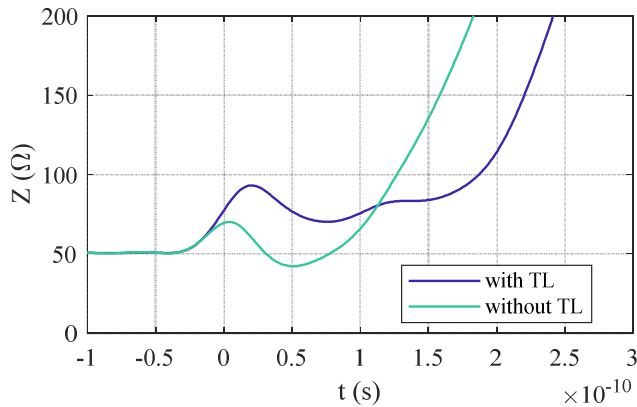


Figure 8: TDR measurement of device *B* pins with and without TL with respect to CC-TLP. The impedance increases along the line. The signal delay is about 120 ps.

The stress observed on these pins is paramount to determining the stress that the device can withstand. However, due to the high variability of air discharge CDM testing, it can be difficult to evaluate the difference between testers on these pins after a typical CDM validation test with only three discharges per polarity.

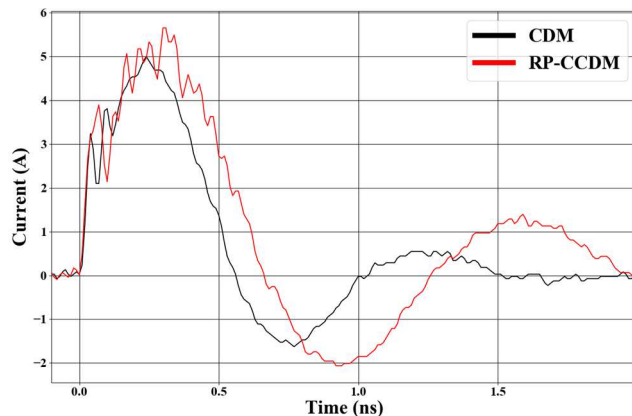


Figure 9: Comparison of CDM and RP-CCDM on transmission line (TL) connected pin of device *B* during qualification test.

C. Peak Current Comparison of Pin Types

To evaluate these pins more accurately, a 100-pulse test was performed by stressing a reference connected pin and a TL pin 100 times each. All testers were tested at a 500 V field charge voltage to prevent any spark differences that may occur if the JS-002 voltage factor method was incorporated. The pogo pins and dielectric surface were cleaned with isopropyl alcohol prior to testing and the testing was performed below 10%

relative humidity to minimize peak variation due to the air spark. Due to the charge distribution over the whole chip and high current levels with ESD devices operating in the on-state, no difference is expected in the discharge waveforms from before failure to after failure of the device. An additional CDM tester head with a replaceable pogo pin was incorporated to evaluate the influence of various pogo lengths on the observed discharge peak. This new test head was used alongside the RP-CCDM and CDM heads used in all device testing. The CDM head used for device testing is indicated as “large diameter” since it has a diameter of 1.5 mm compared to the new test head’s 0.4 mm pogo diameter. Table 2 displays the maximum peak current measured within the 100-pulse test for each setup and the relative percentage of the TL pin peak current to the reference connected pin peak current.

Table 2: Maximum current captured on each pin during a 100-pulse test and the resulting current ratio of the pins.

	Pogo length (mm)	GND peak current (A)	High speed I/O peak current (A)	Peak current percentage I/O/GND (%)
CDM (Large Dia.)	6.1	7.84	5.66	72.2
CDM	4.2	8.16	6.30	77.2
CDM	6.6	6.76	5.44	80.5
CDM	10.7	5.79	4.69	81.0
ACRP-CCDM	13.2	6.48	5.05	77.9
RP-CCDM	13.2	6.44	5.35	83.1

As can be seen in Table 2, there is a correlation between the length of the pogo pin and the discharge current ratio between the TL connected pin and the GND pin. For a given pre-charge voltage (with voltage factors applied such that the RP-CCDM and CDM peak currents match on JS-002 verification modules) where a CDM stress induces 5 A peak current on the studied TL pin, the RP-CCDM stress will induce a 5.7 A peak current. This additional current can be clearly seen

in the measured currents shown in Figure 9, which was taken during a qualification test of device B. The cause of the increased peak current of RP-CCDM with respect to CDM for the same pre-charge voltage on TL pins can be explained by the input impedance of the CDM head. Figure 10 displays the input impedance of the CDM heads used in Table 2 as measured in [6], denoted as Z_{DUT} . Due to higher input impedance in the 600 MHz to 2 GHz range, where the majority of the spectral content is contained (Fig. 5), a larger reflection back into the device trace will occur in the case of the RP-CCDM. As discussed in [12, 13], the stress the die experiences is a result of the reflected pulse off this discontinuity. As a result, the stress a TL connected I/O receives will be greater for a CDM head with a higher input impedance, given a matching peak amplitude on a calibration coin.

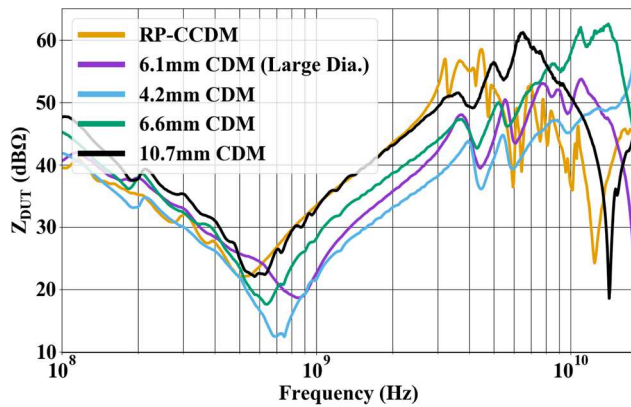


Figure 10: Measured Z_{DUT} of CDM heads used in transmission line pin 100 pulse test. Increased pogo pin inductance can be observed as a left and upward shift in the positive sloping region. This results in a higher impedance at the pogo-pin/device-pin interface.

D. Simulation of Transmission Line Pins using Z_{DUT}

To determine if the measured Z_{DUT} values alone could predict the difference, a simulation using the measured Z_{DUT} data was done in ADS by Keysight. A simplified circuit model, developed in [12], was adopted to represent a CDM event on a TL pin where the current must travel through the impedance-controlled trace and encounter an impedance discontinuity at the pin/pogo-pin interface.

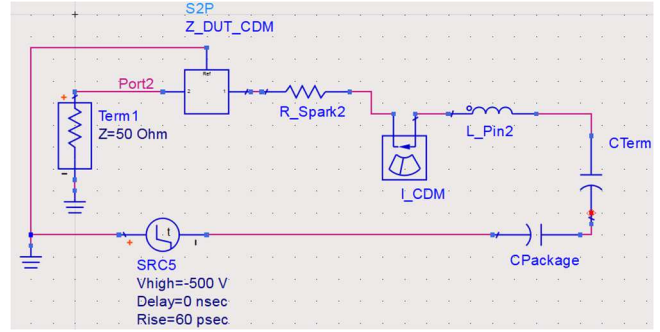


Figure 11: ADS circuit model for reference pin discharge using Z_{DUT} measurement representation of the CDM head

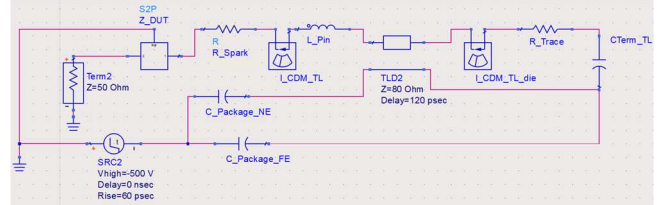


Figure 12: ADS circuit model for transmission line connected pin discharge using Z_{DUT} measurement representation of the CDM head.

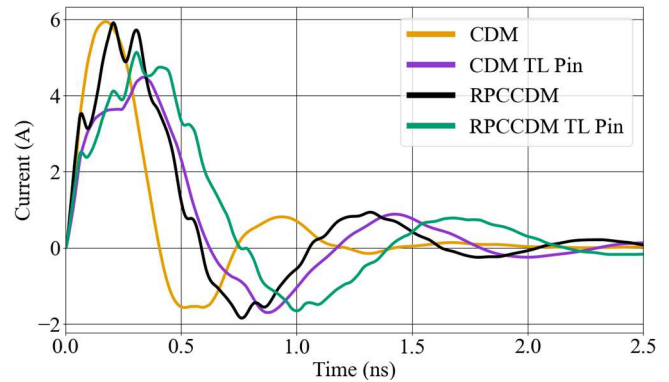


Figure 13: ADS simulation results for transmission line and reference pins.

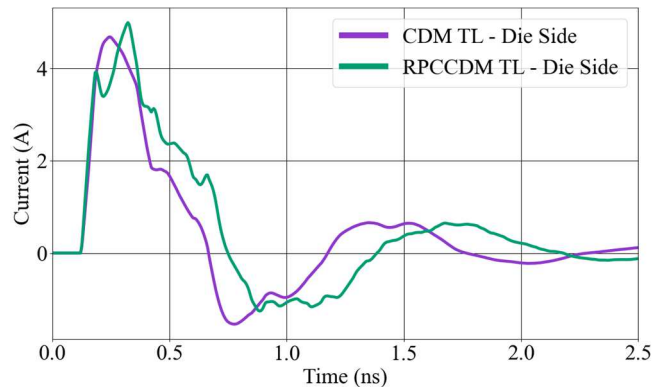


Figure 14: ADS simulation results for comparison of the current on the die side of the transmission line.

As can be seen in Figure 13, the ADS simulation produces the same relationship in measured current as the measured data. The current

measured using the measured RP-CCDM Z_{DUT} to represent the test head structure results in a higher current measurement on the TL connected pin. Figure 14 shows the current measured on the die side of the transmission line and indicates an increased current peak with the RP-CCDM head. Further development with a less simplified model of the TL pin case is necessary to determine the precise stress difference that occurs due to this effect.

IV. Failure Analysis Results

A. Device A Failure Results

Device A was tested using RP-CCDM, CDM, and CC-TLP testers. To test if that the failure levels of device A are risetime dependent, CC-TLP tests were performed using 100 ps and 300 ps risetimes. The determined failure levels of the device A are shown in Table 3 and Table 4. The devices were stressed at increasing test conditions until failure. The recorded withstand current indicates the highest current that all tested devices were able to withstand. Failure analysis on device A was carried out via DC leakage testing.

Table 3: CDM Failure Levels of Device A.

Tester	Test Condition (TC)	Pass/Fail
RPCCDM Factor: 1.10	625	Pass
	750	Fail
CDM Factor: 0.89	625	Pass
	750	Fail

Table 4: CC-TLP Failure Levels of Device A [10].

Tester	Peak current (A)	ESDEMC Pass/Fail	IFX Pass/Fail
CCTLP 100 ps	7 ($\approx$ TC625)	Pass	Pass
	8 ($\approx$ TC750)	Fail	Fail
CCTLP 300 ps	7	Pass	Pass
	8	Fail	Fail

Table 3 and Table 4 display the failure levels for the device A. The RP-CCDM and CDM were observed to correlate well on this device, inducing failures at TC750. Additionally, CC-TLP setups at ESDEMC and IFX both induced failure at 8 A. Figure 15 displays a comparison of each tester's discharge waveforms recorded at the failure threshold of device A. As seen in Figure 16, a clear

jump in the leakage current is evident for each device stressed at its failure threshold.

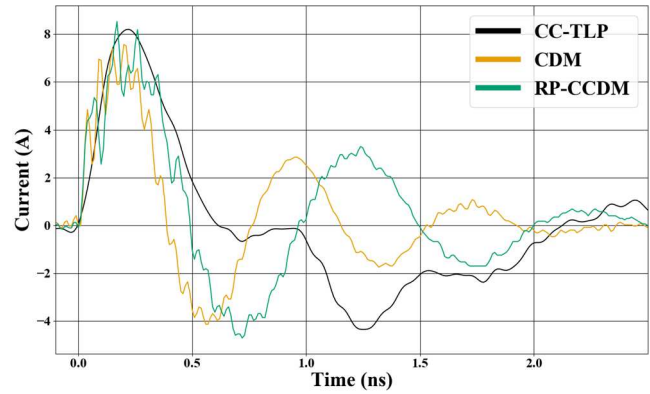


Figure 15: Measured discharges on a sensitive I/O pin on device A for CC-TLP, CDM, RP-CCDM at the 8 A and TC750 test condition, respectively.

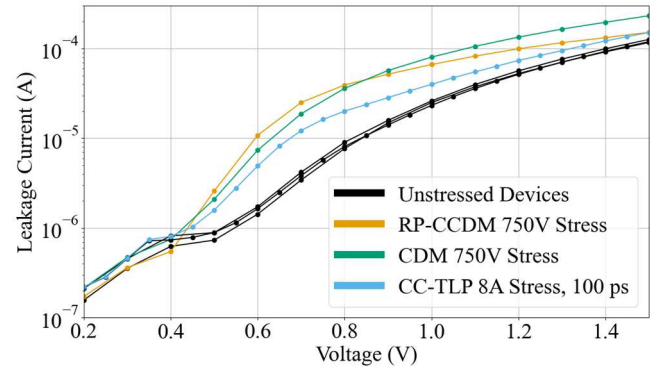


Figure 16: Measured leakage of device A, before and after RP-CCDM and CDM stresses at TC750.

B. Device B Failure Results

Device B was tested with the RP-CCDM and ACRP-CCDM at test conditions of 400 V, 500 V, and 625 V. Additionally, tests with CC-TLP setups were performed at 4 A, 5 A, and 6 A with a 100 ps risetime and 6 A, 7 A, and 8 A with a 300 ps risetime.

Failure analysis on device B is carried out via DC leakage testing and verified via IDDQ testing. The failure is expected for pre-charging voltages higher than TC500 on CDM and located on the edge of the digital core. The IDDQ analysis measures the current consumption in the quiescent state on 200 vectors in the digital core.

The quiescent current into VDD for all vectors is below 100 μ A in case of an unstressed reference device. Slight deviations in this range are traced back to normal variations. A significant increase

of the current compared to the reference device indicates a gate-oxide failure on the edge of the digital core. Significant deviations between vectors in the IDDQ sweep are also an indication of failure on the edge of the digital core.

Table 5 and Table 6 display the failure levels for device B. Figure 17 - Figure 20 display the IDDQ readouts indicating the failure thresholds for each tester.

Table 5: CDM Failure Levels of Device B

Tester	Test Condition (TC)	Pass/Fail
RPCCDM Factor: 1.10	400	Pass
	500	Fail
	625	Fail
ACRPCCDM Factor: 1.10	400	Pass
	500	Fail
	625	Fail
CDM Factor: 0.89	500	Pass
	625	Fail

Table 6: CC-TLP Failure Levels of Device B

Tester	Test Condition (A)	ESDEMC Pass/Fail	IFX Pass/Fail
CCTLP 100 ps	4 ($\approx$ TC400*)	Pass	Pass
	5 ($\approx$ TC500*)	Fail	Fail
	6	Fail	Fail
CCTLP 300 ps	6	Pass	Pass
	7	Pass	Pass
	8	Fail	Fail

* RP-CCDM Stress

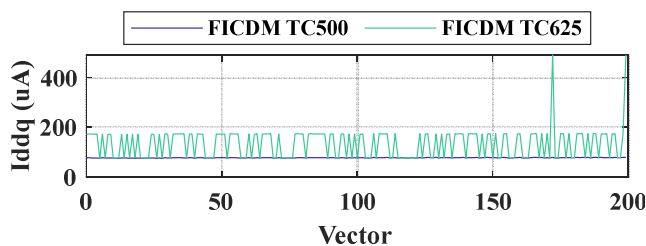


Figure 17: IDDQ analysis of a FICDM stressed device showing increased current consumption indicating failure at TC625.

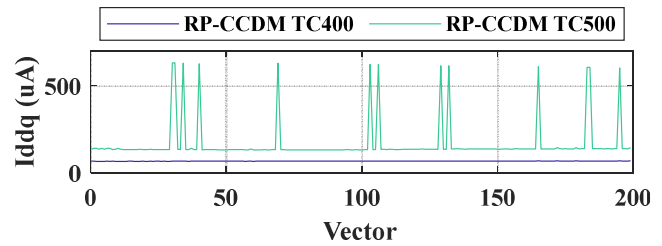


Figure 18: IDDQ analysis of a RP-CCDM stressed device showing increased current consumption, indicating failure at TC500.

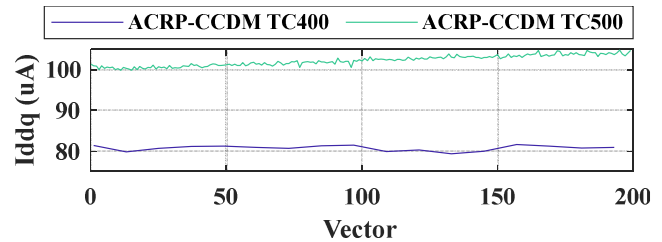


Figure 19: IDDQ analysis of a RP-CCDM stressed device showing increased current consumption, indicating failure at TC500.

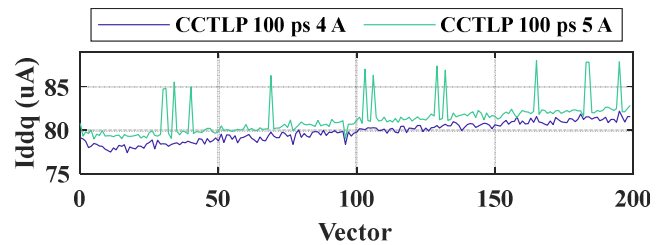


Figure 20: IDDQ analysis of a CC-TLP stressed device showing increased current consumption, indicating failure at 5A.

As shown in Table 5, the RP-CCDM induced failures below the TC500 withstand voltage of the device on a CDM tester. Figure 21 displays the measurement of the largest amplitude stress discharge for the CC-TLP, ACRP-CCDM, and RP-CCDM stress sets at 5 A, TC500, and TC500, respectively.

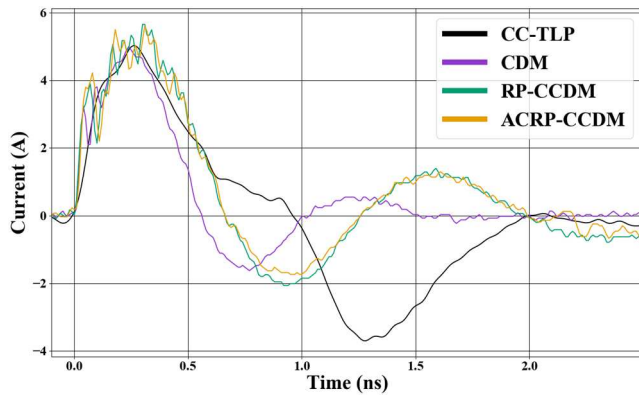


Figure 21: Largest amplitude discharges measured on a sensitive I/O pin on device B for CC-TLP, CDM, RP-CCDM, and ACRP-CCDM at the 5 A and TC500 test condition, respectively.

As shown in Figure 21, the ACRP-CCDM and RP-CCDM have similar pulse shapes and amplitudes on the sensitive I/O pin studied previously and produce failures at the same test condition. The RP-CCDM IDDQ sweep shows a more larger failure, which may be due to the more controlled spark environment and therefore slightly higher peak currents. Both the RP-CCDM and ACRP-CCDM testers produce increased amplitude pulses on TL pins when compared to the CDM tester due to the higher input impedance as discussed in detail in section III. The failure of both the ACRP-CCDM and RP-CCDM to correlate to the CDM at TC500 indicates that the geometry of the test head is likely responsible for the early failures on device B, rather than the spark event in the relay environment. The geometry contributes to a higher stress in the case of ACRP-CCDM and RP-CCDM due to the TL pin effect studied in section III.

As shown in Table 6, the peak current failure thresholds of both CC-TLP testers correlated well with each other by producing repeatable failures at 5 A peak current with a 100 ps risetime pulse and at 8 A with a 300 ps risetime pulse. It was observed during the correlation study that a failure at 5 A could not be reliably achieved until the risetime of the incident TLP pulse at the CC-TLP probe port was slightly decreased and approached 90 ps on the ESDMC tester. This observation reasserts that the risetime of the stress is a critical stress parameter of device B and that the exact risetime of the incident TLP pulse is an important factor to consider when correlating CC-TLP systems.

V. Conclusions

In this study, the RP-CCDM test method was evaluated in comparison to the CDM and CC-TLP test methods using high bandwidth measurement and spectrum analysis, input impedance measurement and circuit modeling on TL pins, and device failure analysis on two devices.

It was shown that a longer pogo pin can induce a larger amplitude current discharge on a TL pin, given a matched peak current on a reference pin, due to the larger input impedance seen at the pogo-pin/device pin interface. This effect was replicated using a simplified model in ADS.

The RP-CCDM showed perfect correlation to CDM stress tests on one device, but consistently showed failures at a lower threshold on a second device. Although construction and excitation sources of both CC-TLP testers are different, they correlated well with the failures induced by the CDM and were helpful in indicating whether risetime was a critical stress parameter of the test devices.

The RP-CCDM was also used to perform air discharge tests, when the relay in the pogo-pin was closed during the entirety of the test and resulted in failure levels that matched RP-CCDM results. These results indicate that the RP-CCDM structure is likely responsible for the early failures on the second device due to the increased currents induced on TL pins. Analysis of the spectra between CDM (air spark) and RP-CCDM (relay spark) suggest that there is no significant increase in spectral content other than that caused by as more stable, low impedance spark. This observation suggests that the RP-CCDM may represent a “worst-case” air spark, that is the spark that would occur between two very clean surfaces at low relative humidity. More testing and statistical analysis of the RP-CCDM is necessary to make a conclusion about the “worst-case” analogy.

VI. Acknowledgments

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VII. References

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